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赛昉“满天芯”助力RISC-V芯片产业发展

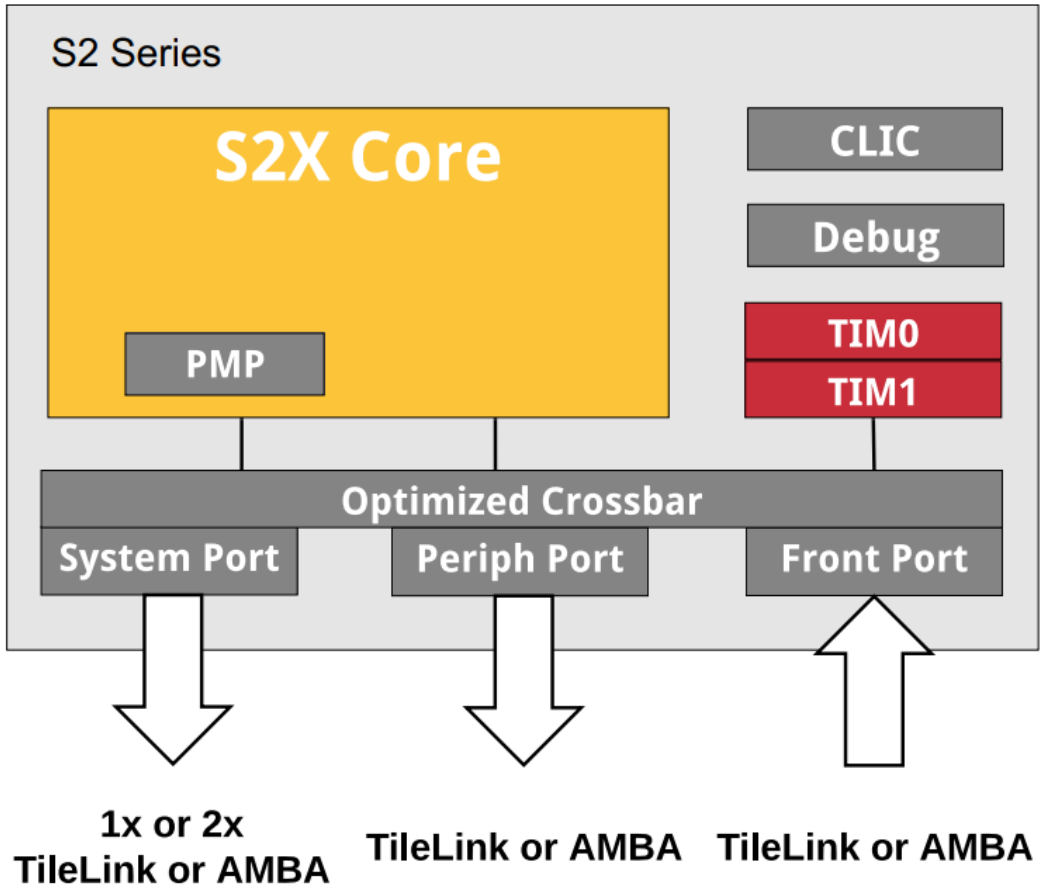
——免费内核S2快速上手

2020年7月15日

- S2系列CPU功能介绍
- S2 免费CPU IP 申请流程
- S2 CPU IP 在线配置
- S2 CPU 开发包组成和快速上手
- S2 CPU 软件开发介绍
- 总结

S2系列CPU功能介绍

- S2 架构简介
  - RV32(E)IMAC
  - 2-3 流水线, 可选哈弗架构
- 有效率的内存访问
  - 可配置数目，且支持业界标准的端口界面
  - 可配置的紧耦合内存访问接口（TIM）
- 中断控制器 (CLIC)
  - 可编程且支持嵌套的硬件中断
  - 最快6 cycle可响应中断
- S2高级版本功能支持
  - 支持cJTAG
  - 支持指令缓存（ucache）
  - 支持指令跟踪（Trace）
  - 支持浮点（RV32FD）
  - 支持RISC-V 用户自定义指令接口
  - 支持RISC-V 未来的指令标准（RV32 B/V/P，规划中）



S2 免费CPU IP 申请流程

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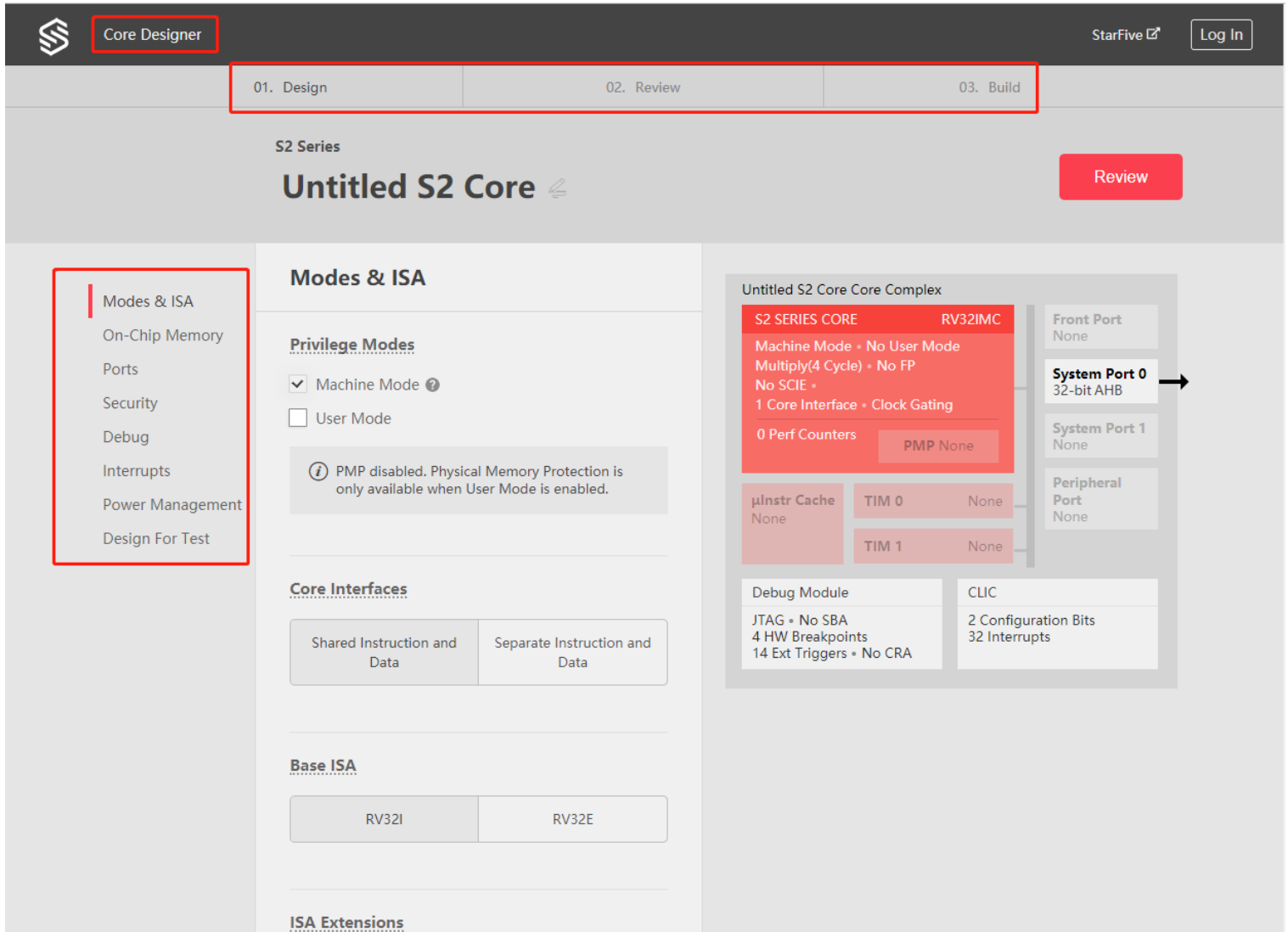
S2 CPU IP 在线配置

http://scd.starfivetech.com/



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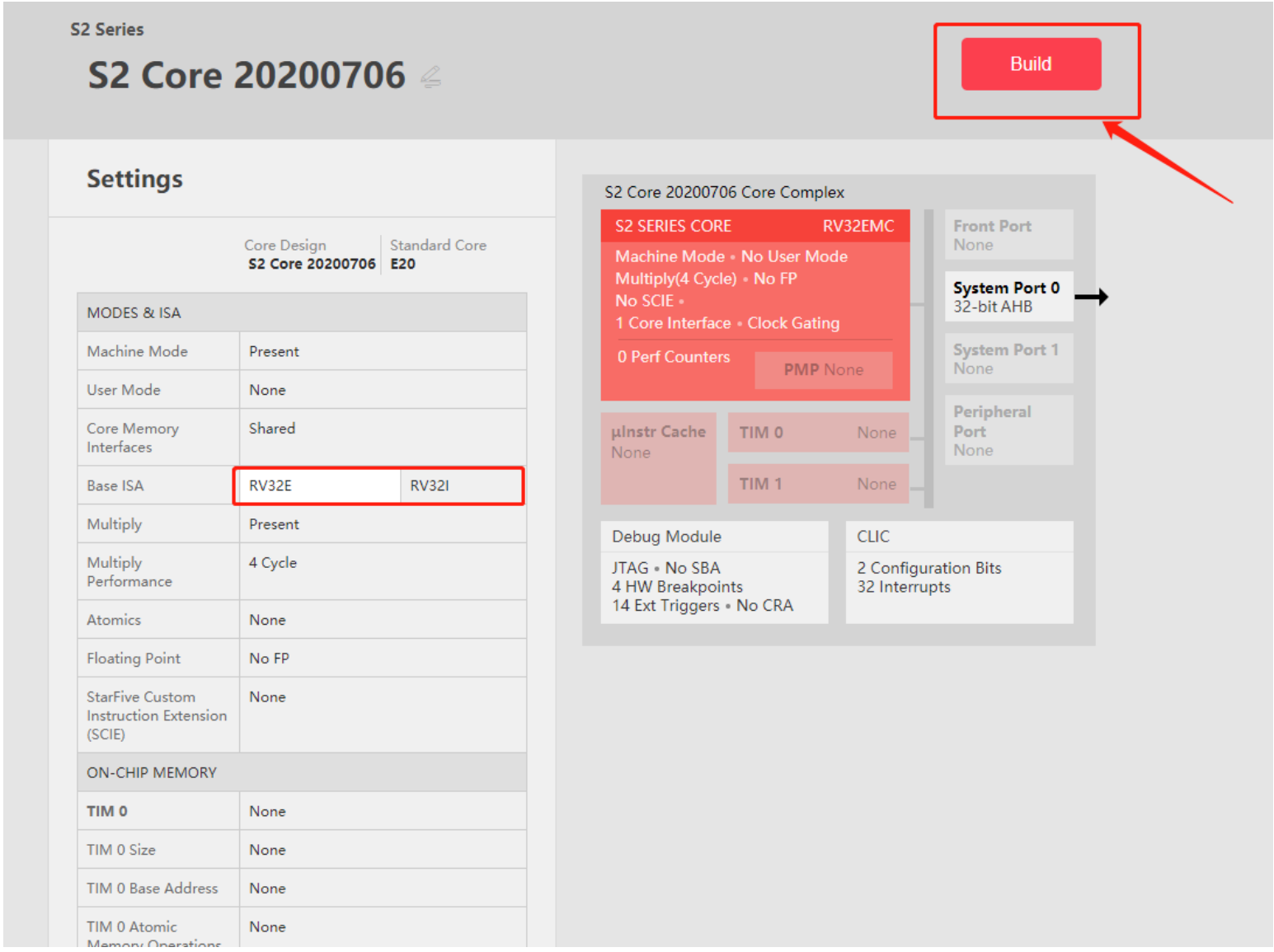

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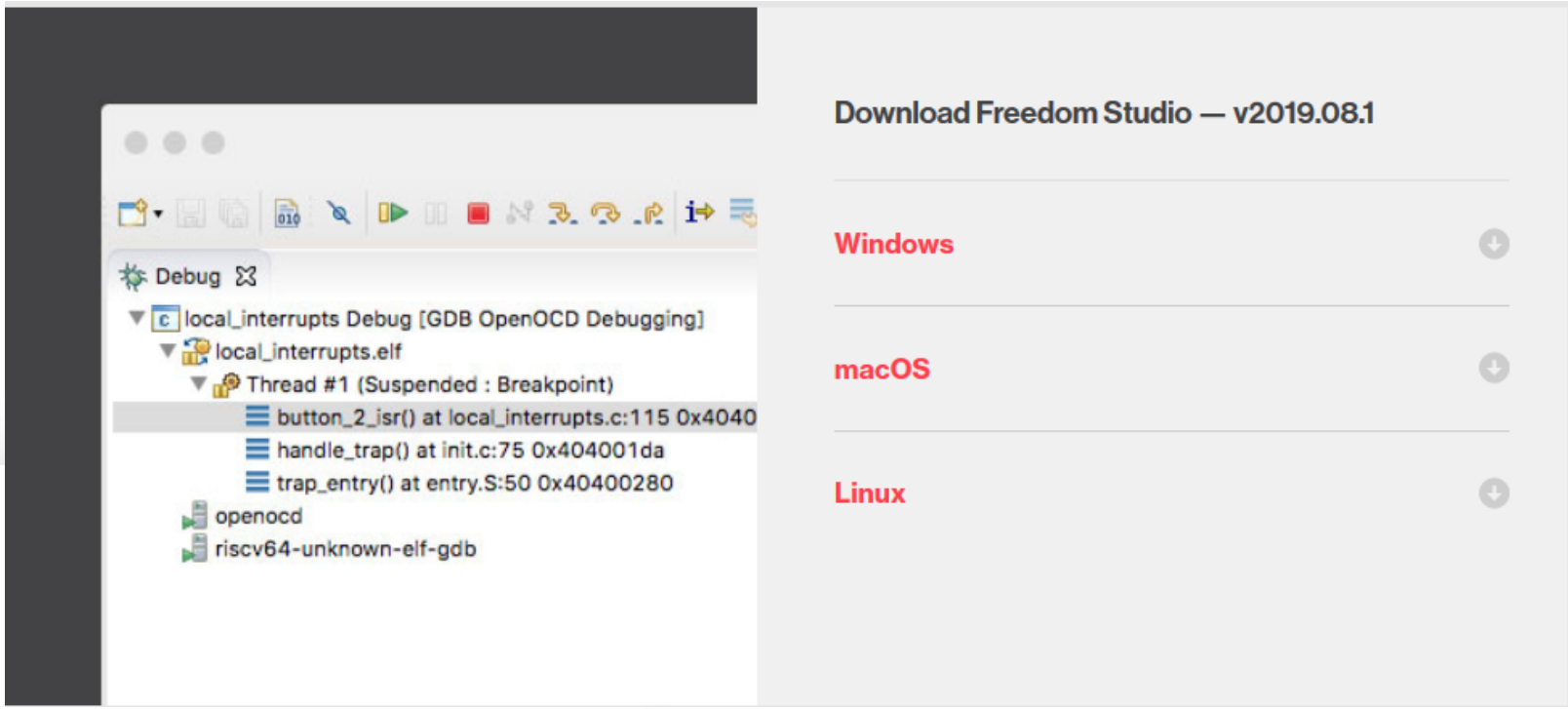
S2 CPU 开发包组成和快速上手

- S2 开发包内容完整：CPU IP RTL + 文档 + Test Bench + FPGA Bit + 软件开发环境
- 开发包快速上手步骤：
  - 开发包已提供仿真脚本，支持VCS，xrun，verilator 等主流RTL仿真工具
  - 提供Insight 模块帮助用户快速调试，用波形图做Debug
  - 提供Freedom E SDK 环境添加并快速编译新的测试用例
- 赛昉科技额外免费提供支持：
  - 参考综合SDC 约束文件
  - 参考综合脚本
  - 仿真环境下的调试接口连接环境
  - 参考集成设计

S2 CPU 软件开发介绍



硬件资源：

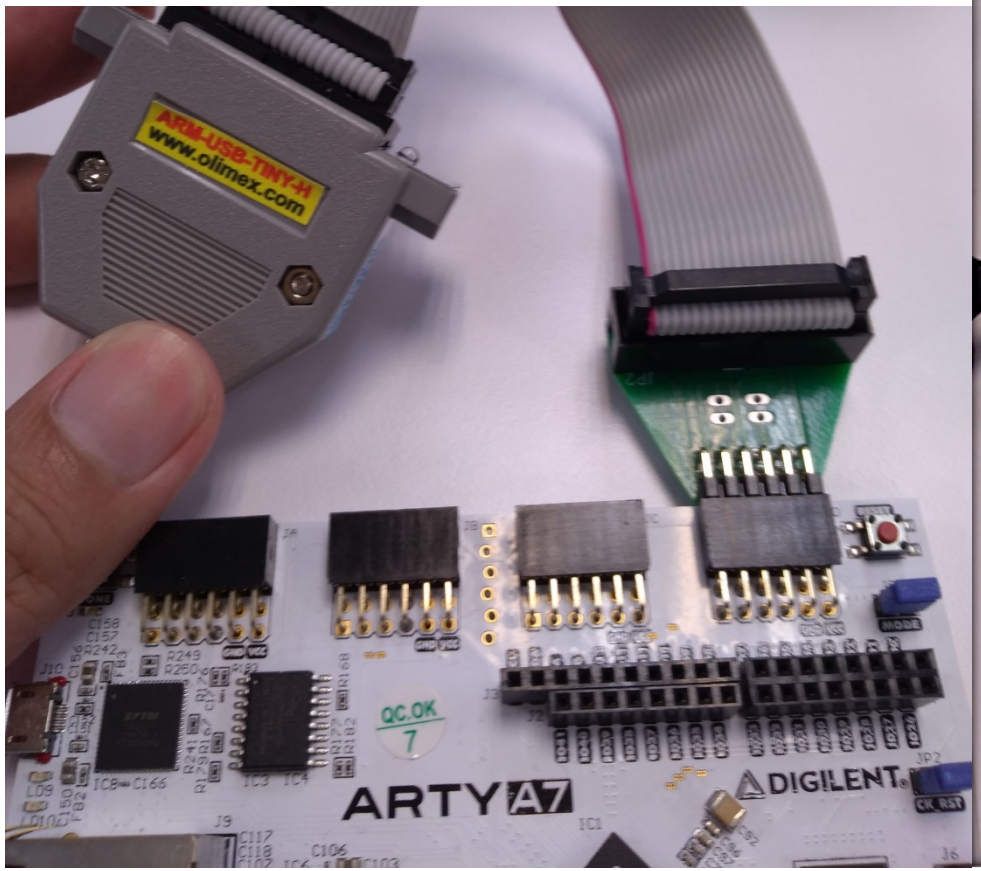
- Digilent ARTY A7主板
- Olimex Debugger
- USB to Micro-USB连接线，用于FPGA 供电和串口打印
- USB TypeA-B cable, 用来连接电脑和调试器

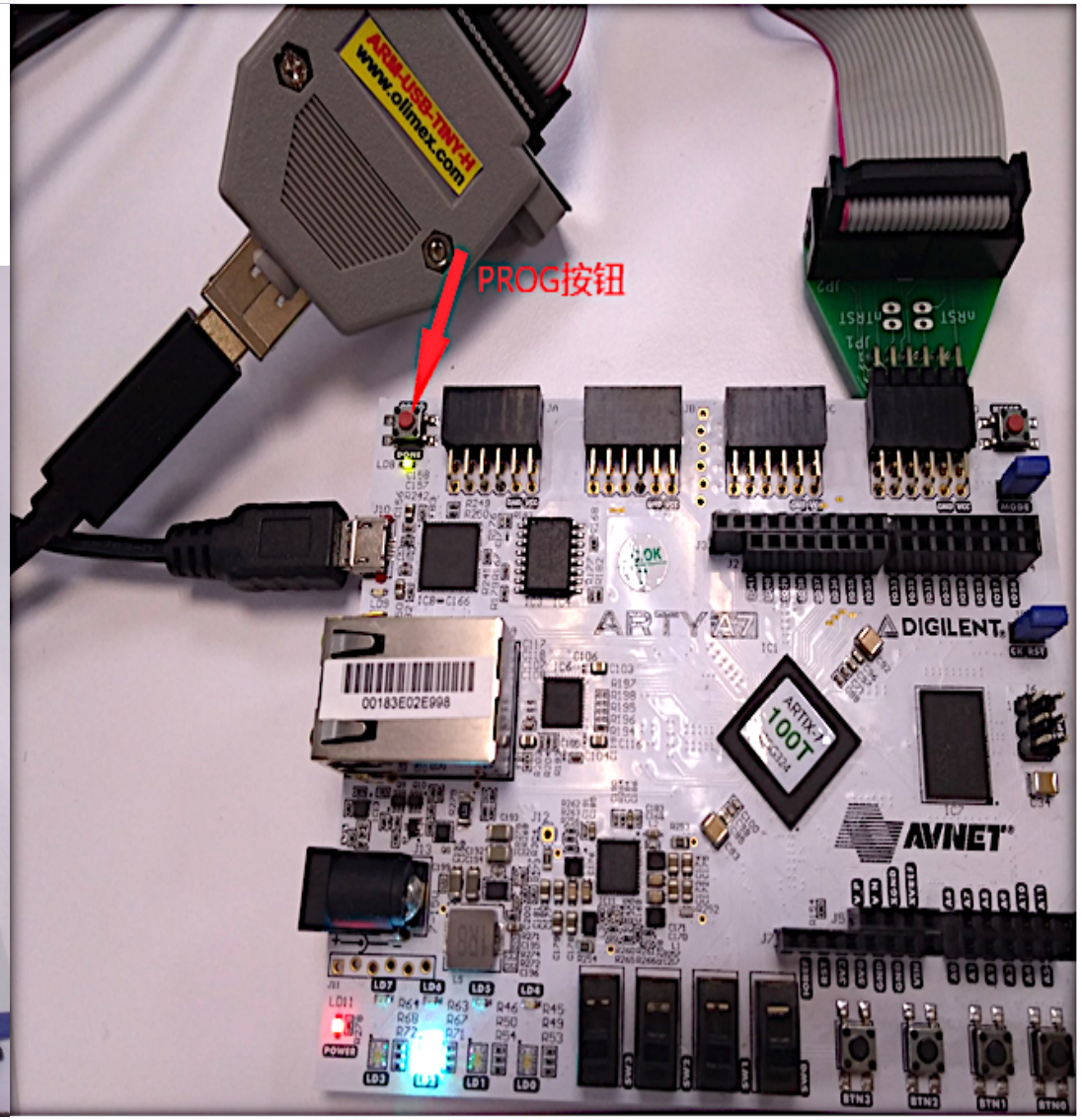
集成开发环境Freedom Studio：

- 下载地址：www.sifive.com/boards

准备FPGA开发板

将您的FPGA开发板，依照下图与Olimex Debugger连接





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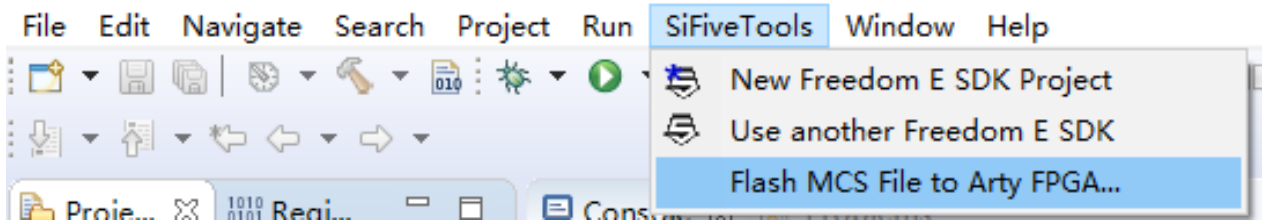
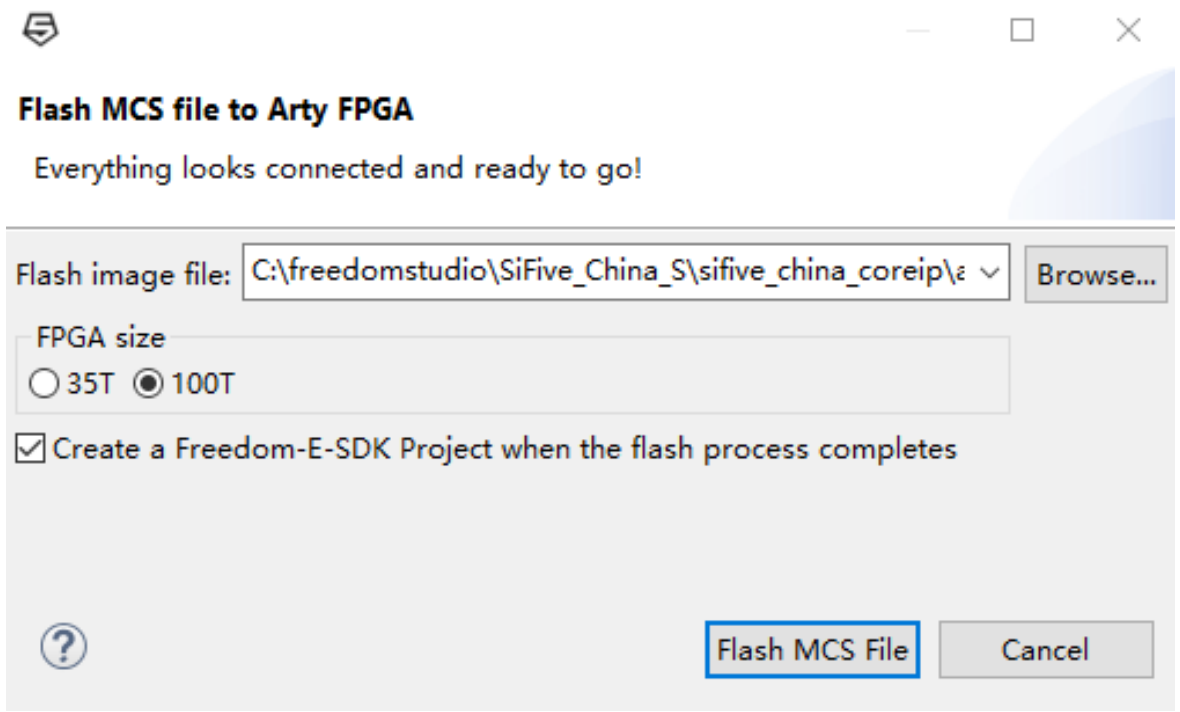
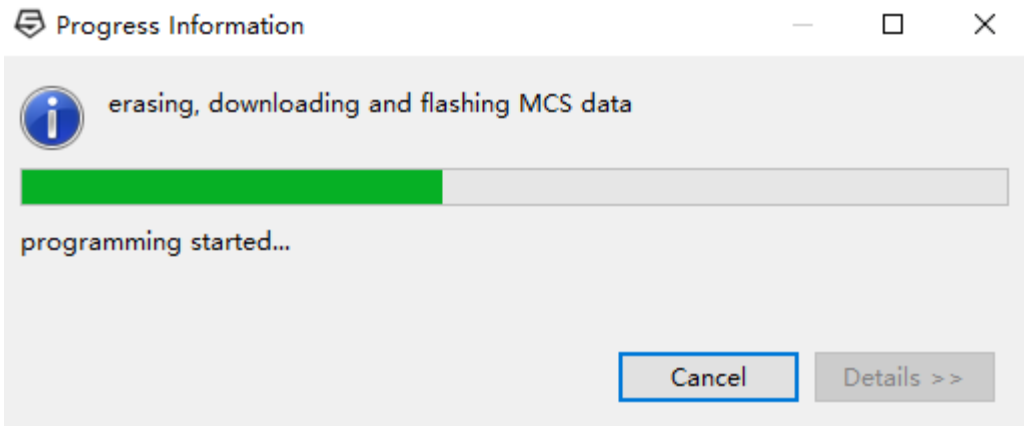
使用Freedom Studio 烧录FPGA开发板



打开Freedom Studio，下载开发包里面的MCS文件到FPGA





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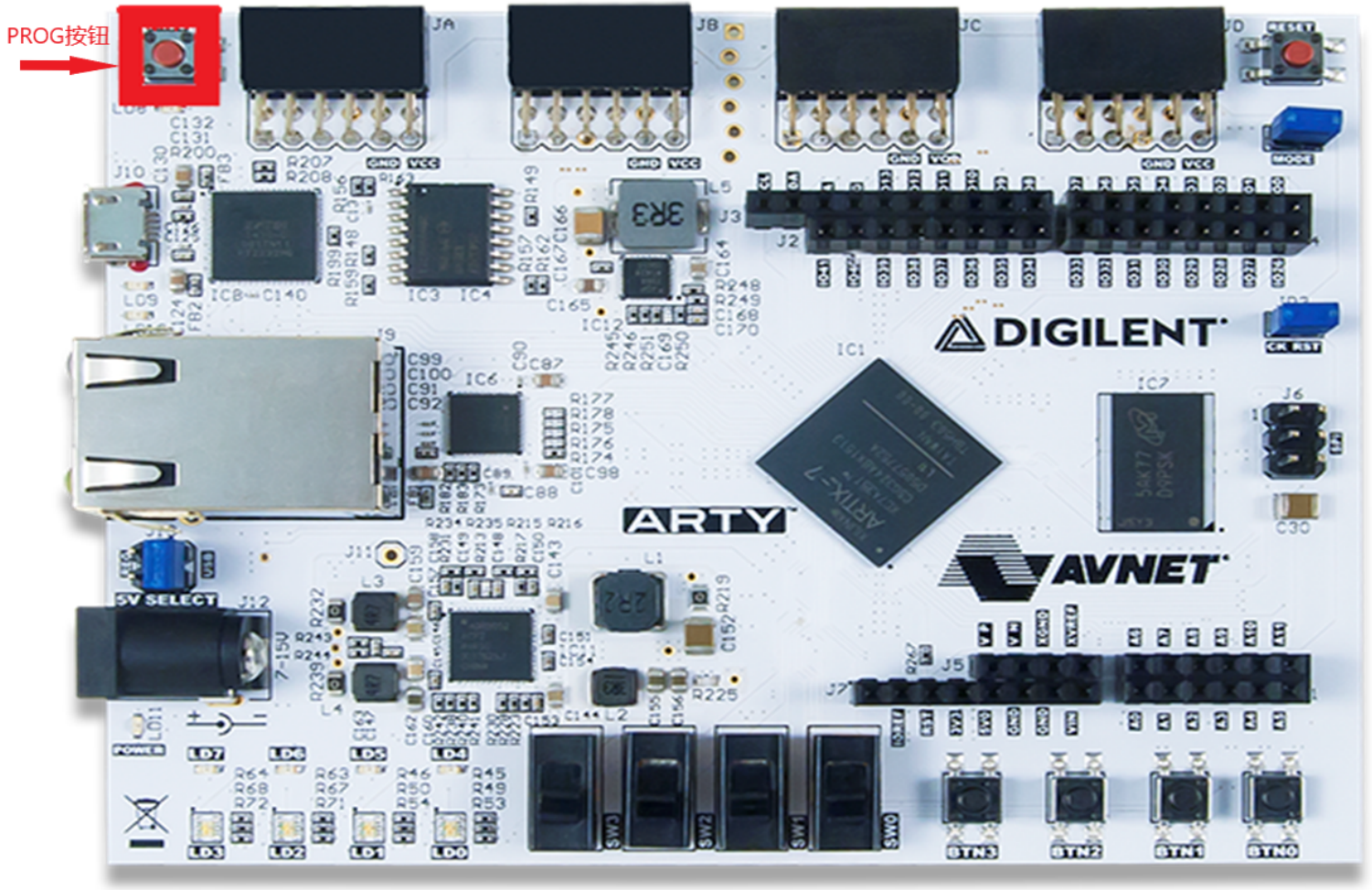
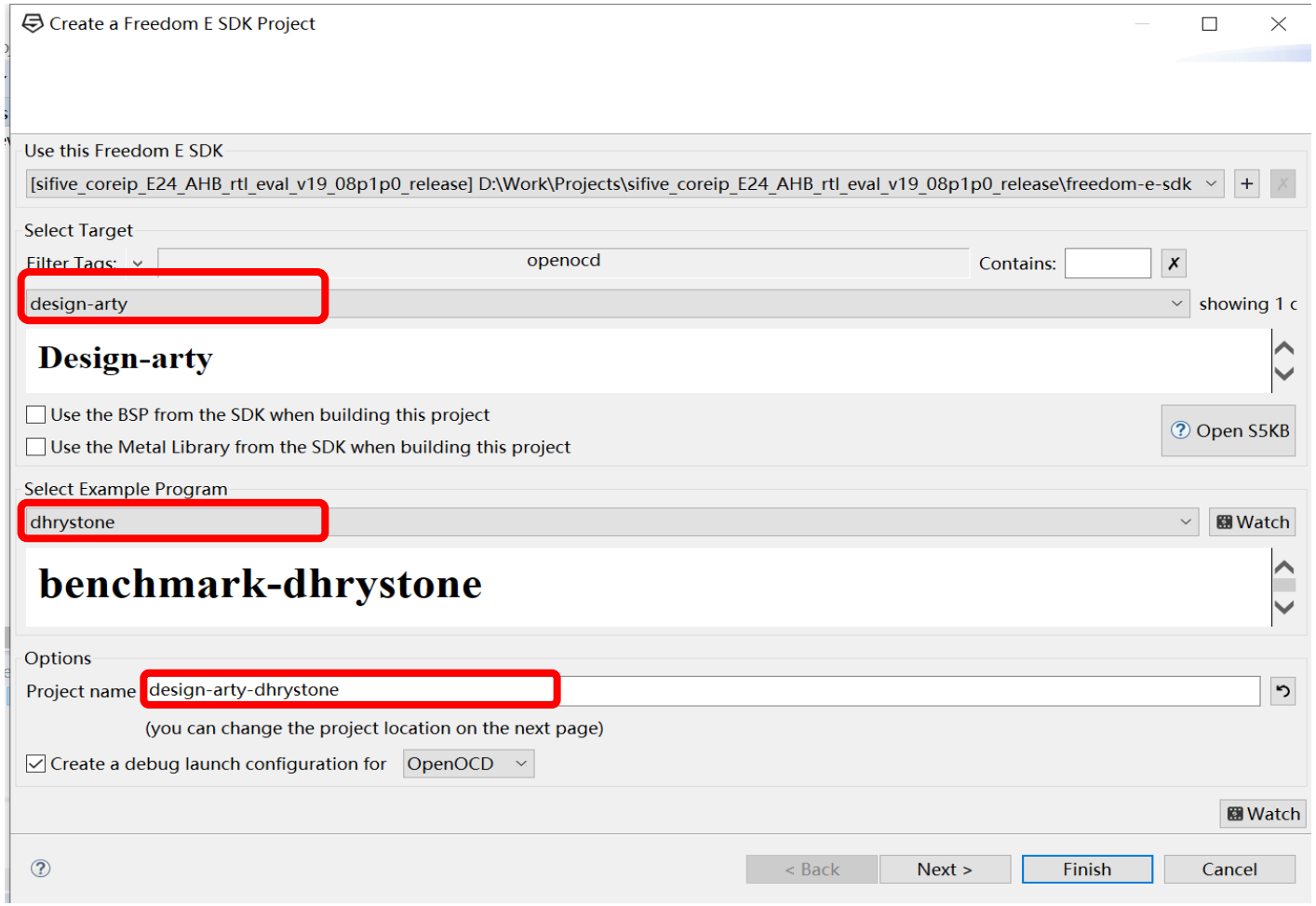
烧录FPGA

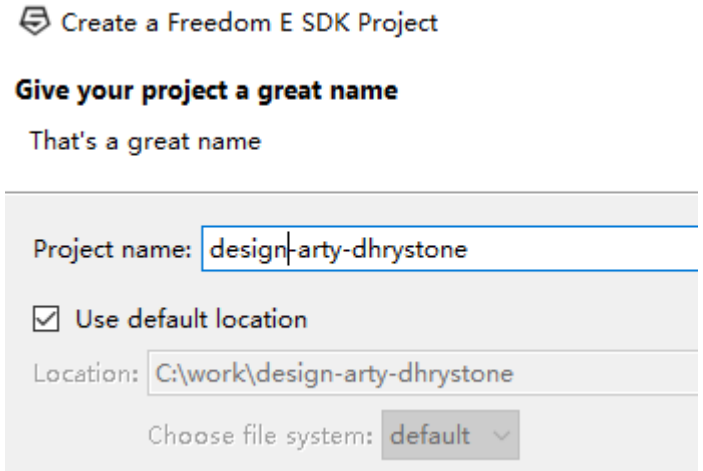
烧录完成，按下PROG键重启FPGA 开发板让网表生效



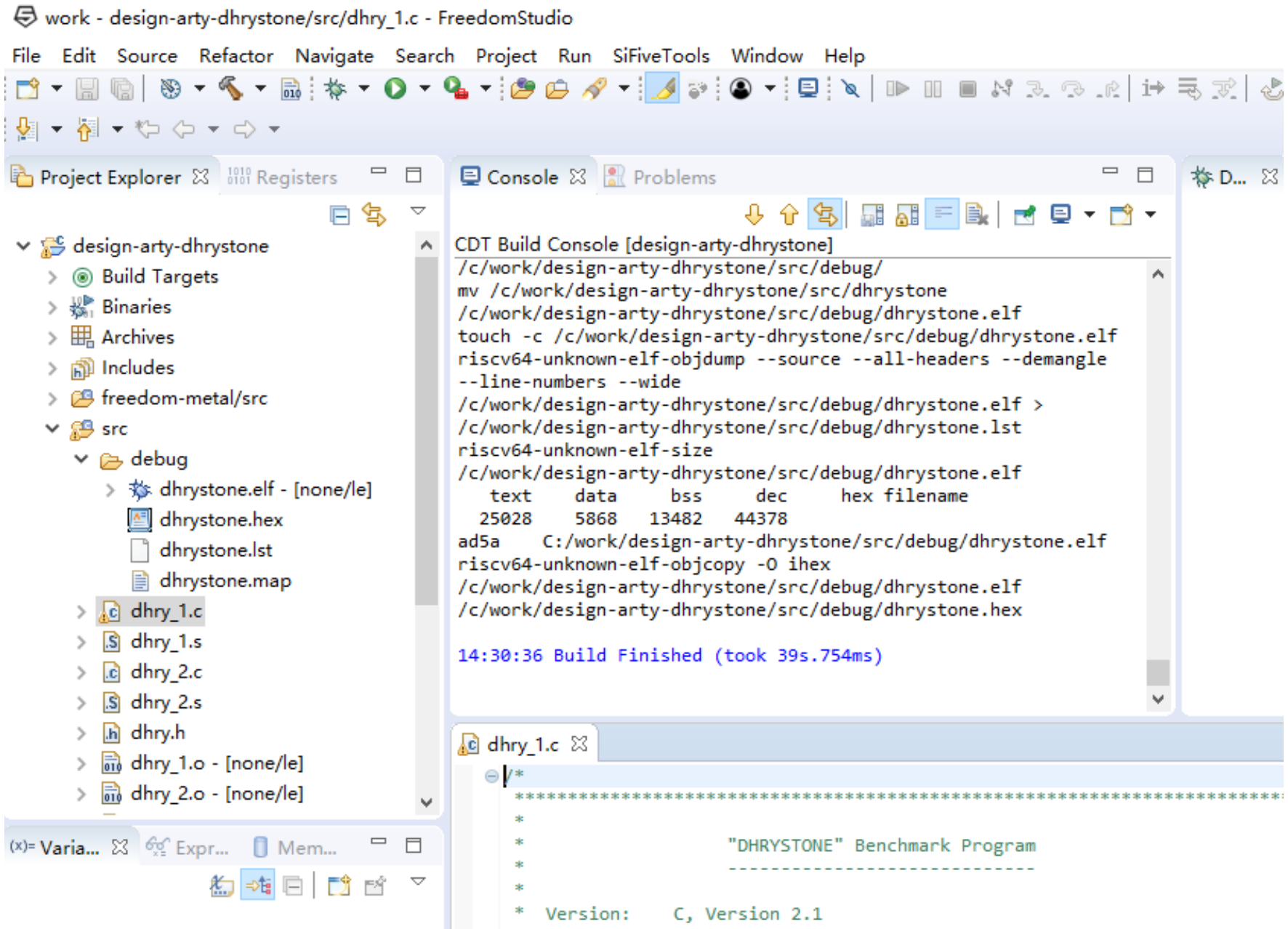
在Freedom Studio中创建工程



- 刻录完成后，Freedom Studio会开始Create Project
  - Freedom Studio 会根据您import的Core IP来Create Project
- 选择您的 Program, 并指定 Project name



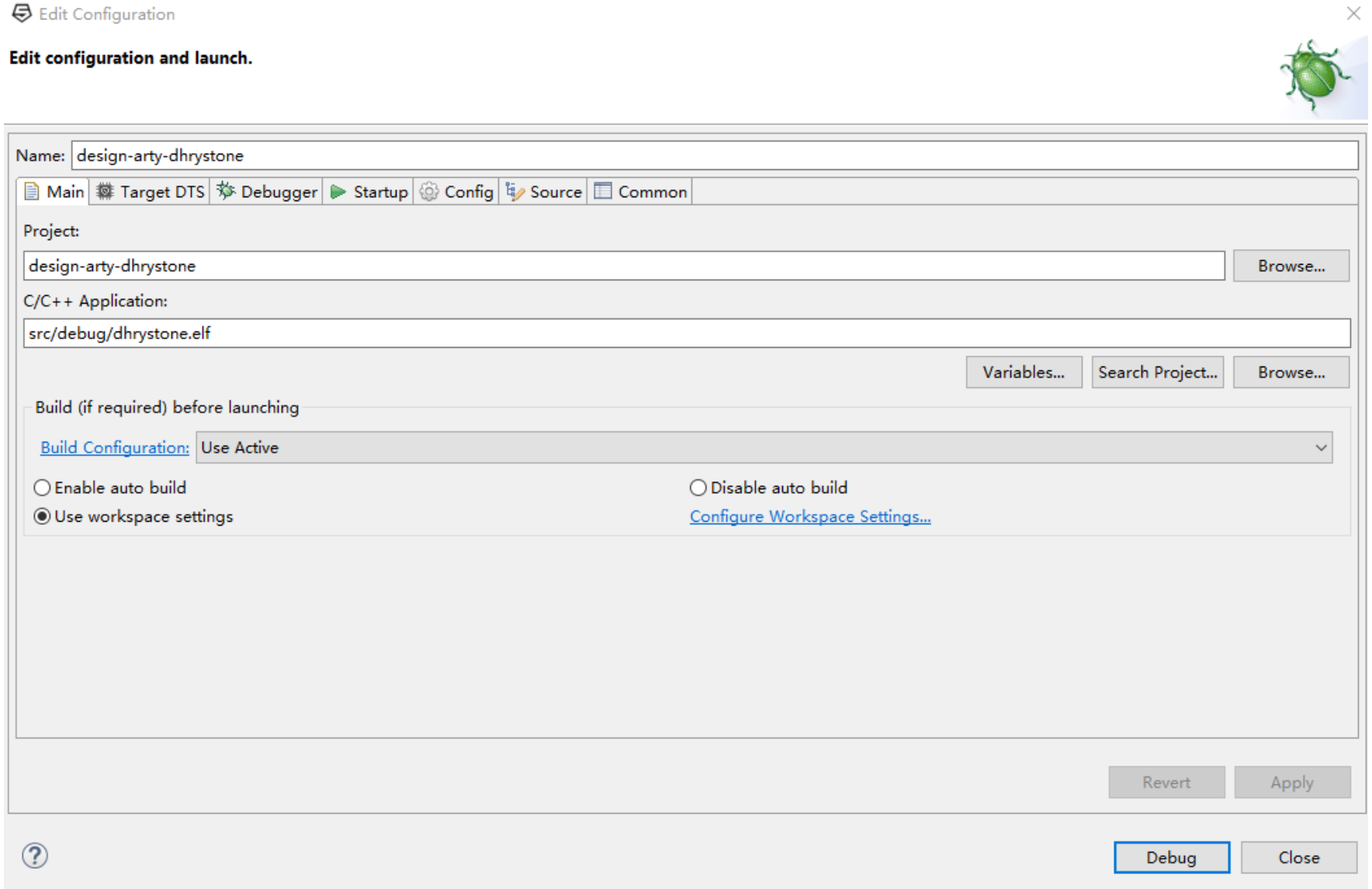
在Freedom Studio中编译工程



建立好Project以后，Freedom Studio会自动开始Build Project

在Freedom Studio中检查配置以运行工程

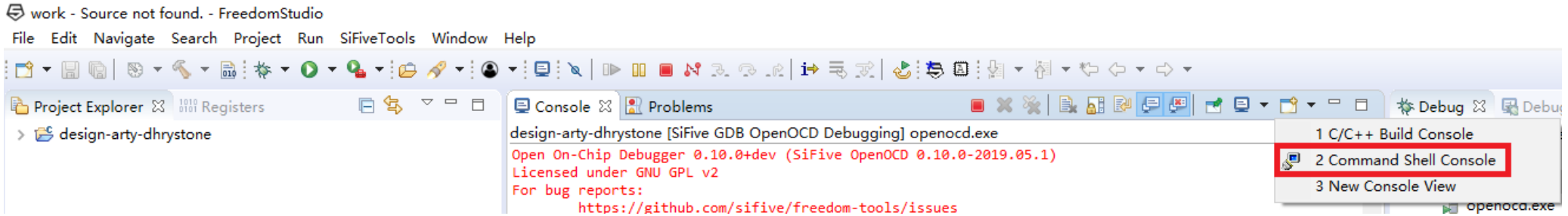
不须选择，直接点选Debug，即可开始Execute Program



在Freedom Studio中打开并配置串口终端视窗

- Configure Serial Port
- Check your device manager to find out the serial port

1



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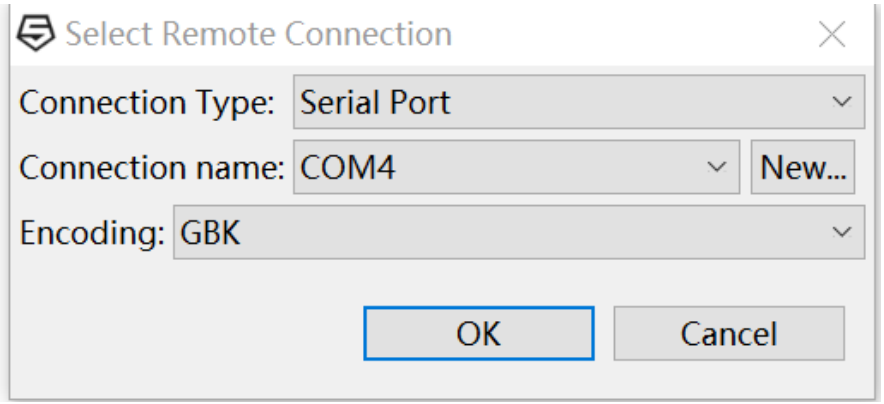

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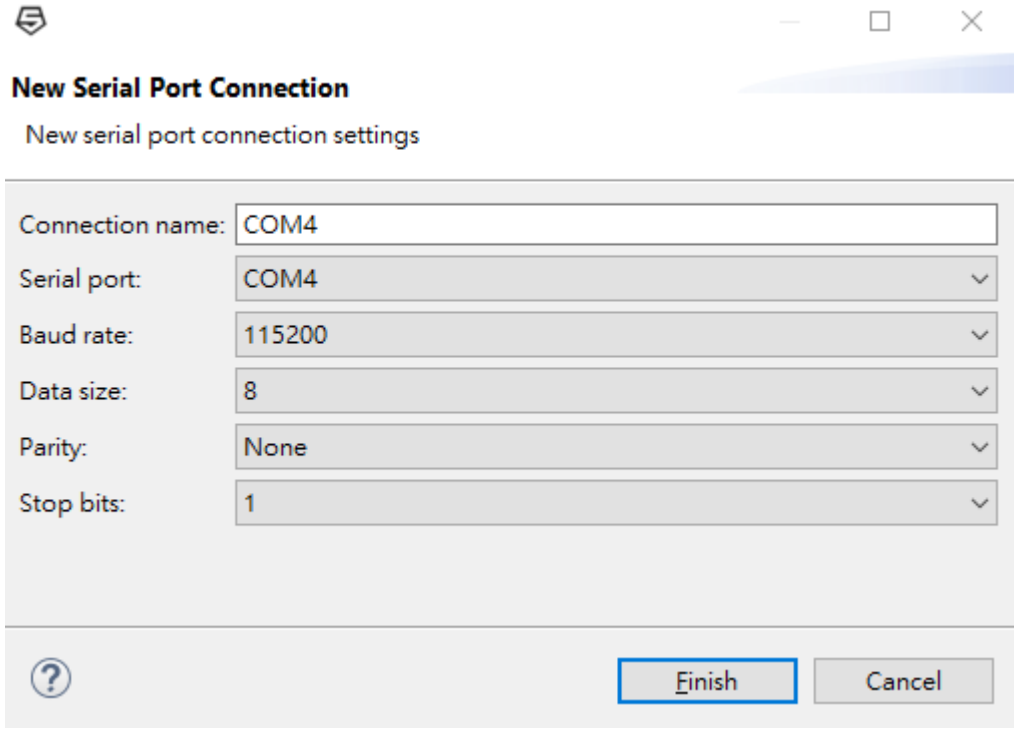

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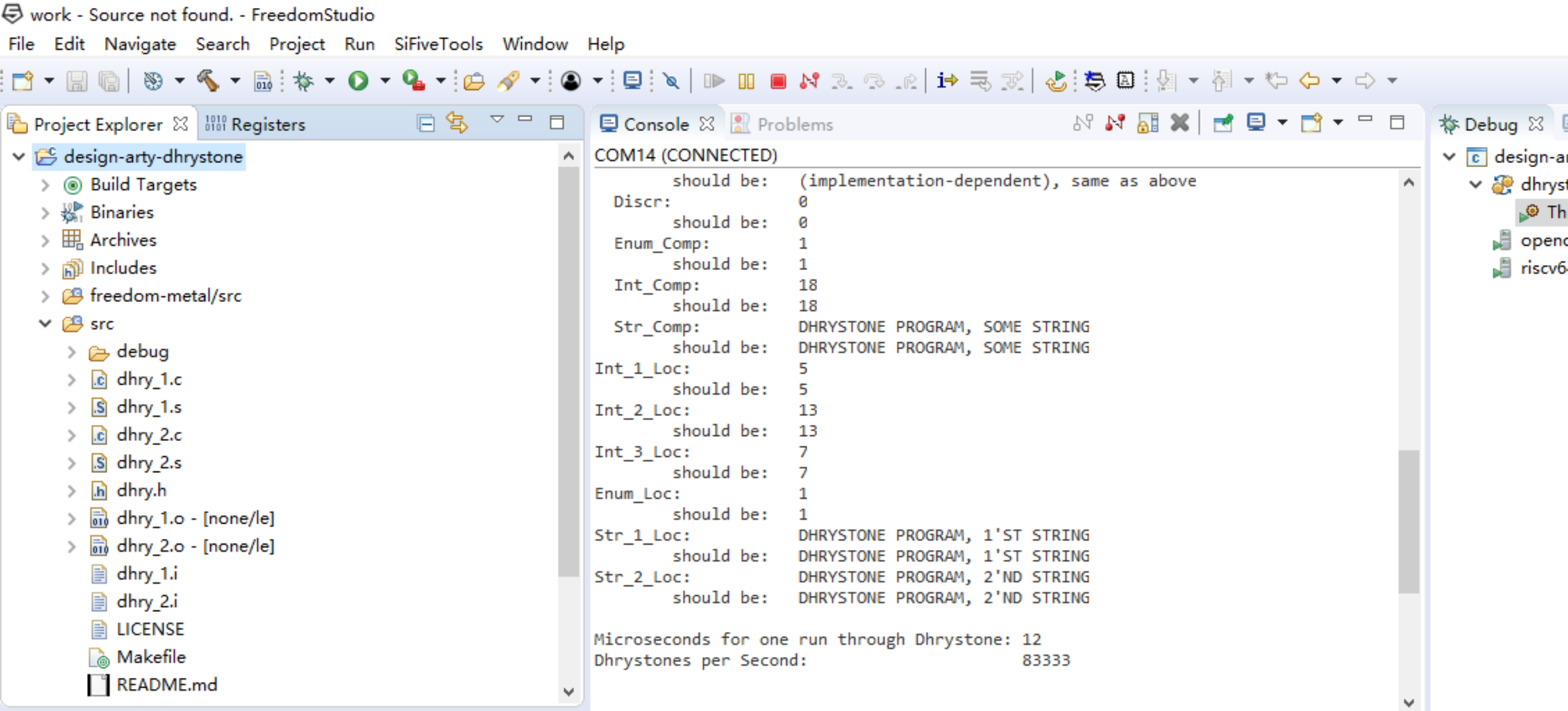
在Freedom Studio中下载程序到FPGA 板并运行

Freedom Studio 会自动执行该program



使用命令行和RISC-V开源工具链运行程序

```
lenovo@LAPTOP-9IIVSE0D C:\Users\lenovo
$ C:\freedomstudio\riscv-openocd-0.10.0-2019.08.2-x86_64-w64-mingw32\bin\openocd.exe -f C:\work\SiFi
ve_China_S\sifive_china_coreip\freedom-e-sdk\bsp\design-arty\openocd.cfg
Open On-Chip Debugger 0.10.0+dev (SiFive OpenOCD 0.10.0-2019.08.2)
Licensed under GNU GPL v2
For bug reports:
        https://github.com/sifive/freedom-tools/issues
adapter speed: 10000 kHz
Info : auto-selecting first available session transport "jtag". To override use 'transport select <t
ransport>'.
Info : ftdi: if you experience problems at higher adapter clocks, try the command "ftdi_tdo_sample_e
dge falling"
Info : clock speed 10000 kHz
Info : JTAG tap: riscv.cpu tap/device found: 0x20000913 (mfg: 0x489 (SiFive Inc), part: 0x0000, ver:
 0x2)
Info : datacount=1 progbufsize=2
Info : Disabling abstract command reads from CSRs.
Info : Examined RISC-V core; found 1 harts
Info :  hart 0: XLEN=32, misa=0x40901105
Info : Listening on port 3333 for gdb connections
Info : Found flash device 'sp s25fl128s' (ID 0x00182001)
cleared protection for sectors 64 through 255 on flash bank 0
Ready for Remote Connections
Info : Listening on port 6666 for tcl connections
Info : Listening on port 4444 for telnet connections
Info : accepting 'gdb' connection on tcp/3333
```

- 需要开启两个console, 一个开启OpenOCD, 另一个开始gdb
- 找到 IP 相对应的 openocd.cfg，即可连接, OpenOCD 会在 port 3333开启 gdbserver
  - 在gdb环境下, 就可以连接 3333 port, 如下页的 target remote :3333

使用命令行和RISC-V开源工具链运行程序

```
lenovo@LAPTOP-9IIVSE0D C:\Users\lenovo
$ C:\freedomstudio\riscv64-unknown-elf-gcc-8.3.0-2019.08.0-x86_64-w64-mingw32\bin\riscv64-unknown-elf-gdb.exe
C:\freedomstudio\riscv64-unknown-elf-gcc-8.3.0-2019.08.0-x86_64-w64-mingw32\bin\riscv64-unknown-elf-gdb.exe: warning: Couldn't determine a path for the index cache directory.
GNU gdb (SiFive GDB 8.3.0-2019.08.0) 8.3
Copyright (C) 2019 Free Software Foundation, Inc.
License GPLv3+: GNU GPL version 3 or later <http://gnu.org/licenses/gpl.html>
This is free software: you are free to change and redistribute it.
There is NO WARRANTY, to the extent permitted by law.
Type "show copying" and "show warranty" for details.
This GDB was configured as "--host=x86_64-w64-mingw32 --target=riscv64-unknown-elf".
Type "show configuration" for configuration details.
For bug reporting instructions, please see:
<https://github.com/sifive/freedom-tools/issues>.
Find the GDB manual and other documentation resources online at:
    <http://www.gnu.org/software/gdb/documentation/>.

For help, type "help".
Type "apropos word" to search for commands related to "word".
(gdb) set architecture riscv:rv32
The target architecture is assumed to be riscv:rv32
(gdb) target remote :3333
Remote debugging using :3333
warning: No executable has been specified and target does not support
determining executable automatically.  Try using the "file" command.
0x8000d920 in ?? ()
(gdb) p/x $pc
$1 = 0x8000d920
(gdb)
```

- 执行gdb, 并依照下列指令顺序, 即可开始debug
- 针对 32 bit RISC-V core, 须设定 set architecture riscv:rv32
- 针对 64 bit RISC-V core, 须设定 set architecture riscv:rv64

总结

- S2 是赛昉科技自主知识产权RISC-V 架构CPU IP，通过“满天芯”计划免费给所有中国企业使用。
- S2 是完全按RISC-V 现有标准实现，包括指令集标准，特权标准，调试跟踪标准。
- S2 提供非常多配置让客户依照需要去选择，赛昉科技提供一个界面友善方便使用的在线RISC-V Core Designer 来用户快速得到最适合的S2 内核。
- S2 开发包内容完整和丰富，用户硬件集成，仿真，综合，物理实现都非常方便，能快速上手。
- S2 软件开发都可以基于RISC-V 现有生态去做，所有生态中的编译器，调试器，集成开发工具，嵌入式实时操作系统， 都可以用于S2 软件的开发。

赛昉科技“满天芯”计划，立足于为国内客户提供全方位的RISC-V服务，助力更多的基于RISC-V的产品上市。让RISC-V满天繁星，璀璨夺目，让RISC-V拥抱未来！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Thank you!