RISC-V Core IP for Target Vertical Markets

SiFive Core IP
Embedding Intelligence Everywhere

Consumer

AR/VR/Gaming devices

Smart Home

Imaging/Wearables

Storage/Networking/5G

SSD, SAN, NAS

Base Stations, Small cells, APs

Switches, Smart NICs, Offload cards

ML/Edge

Sensor Hubs, Gateways

Autonomous machines

IoT devices

SiFive

SiFive

U Cores

64-bit Application Processors

S Cores

64-bit Embedded Processors

E Cores

32-bit Embedded Processors

Embedding Intelligence from the Edge to the Cloud

SiFive

2 Series Core IP:

SiFive's **smallest** and most **efficient** RISC-V processor IP

SiFive

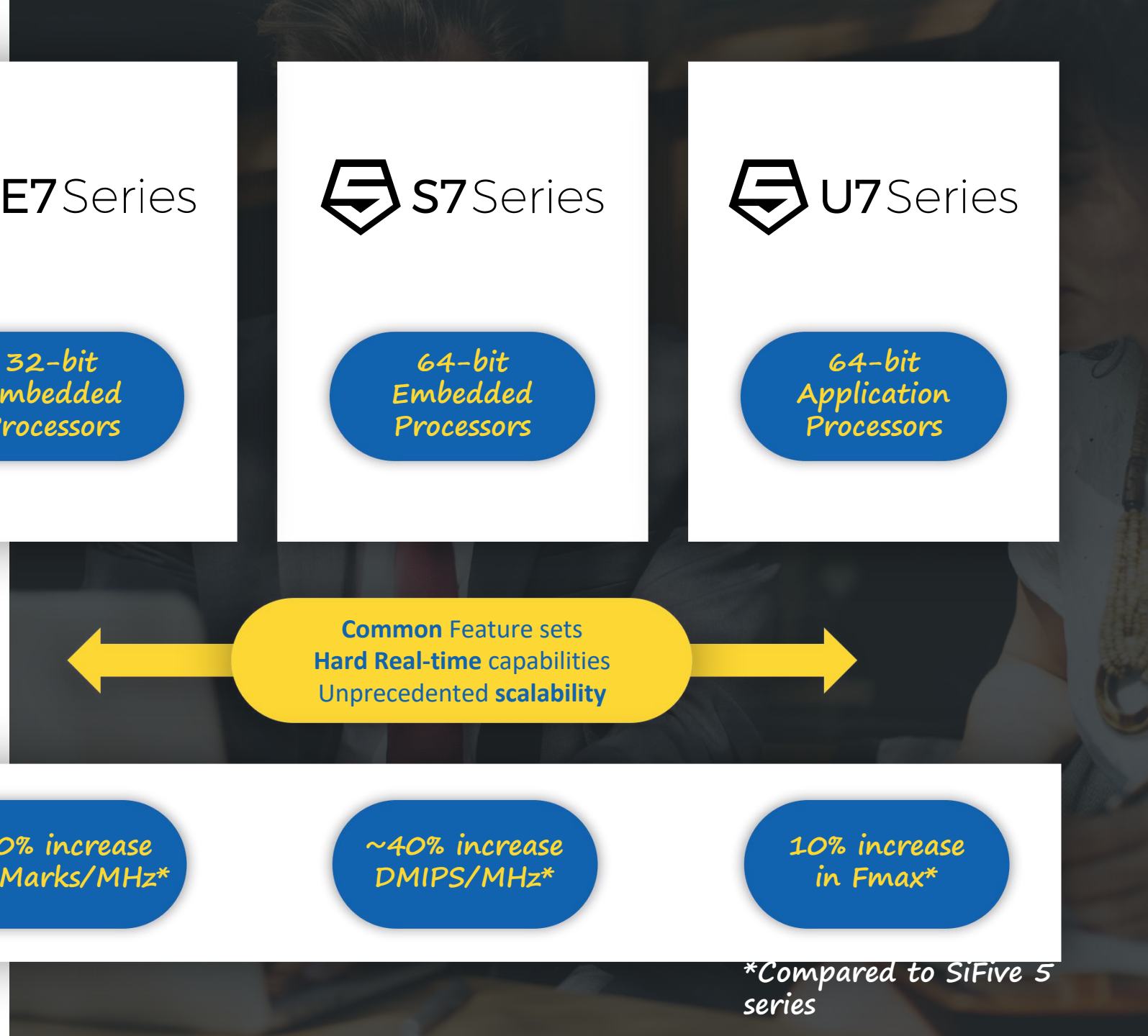
3 & 5 Series Core IP:

The **world's most deployed** RISC-V processor IP

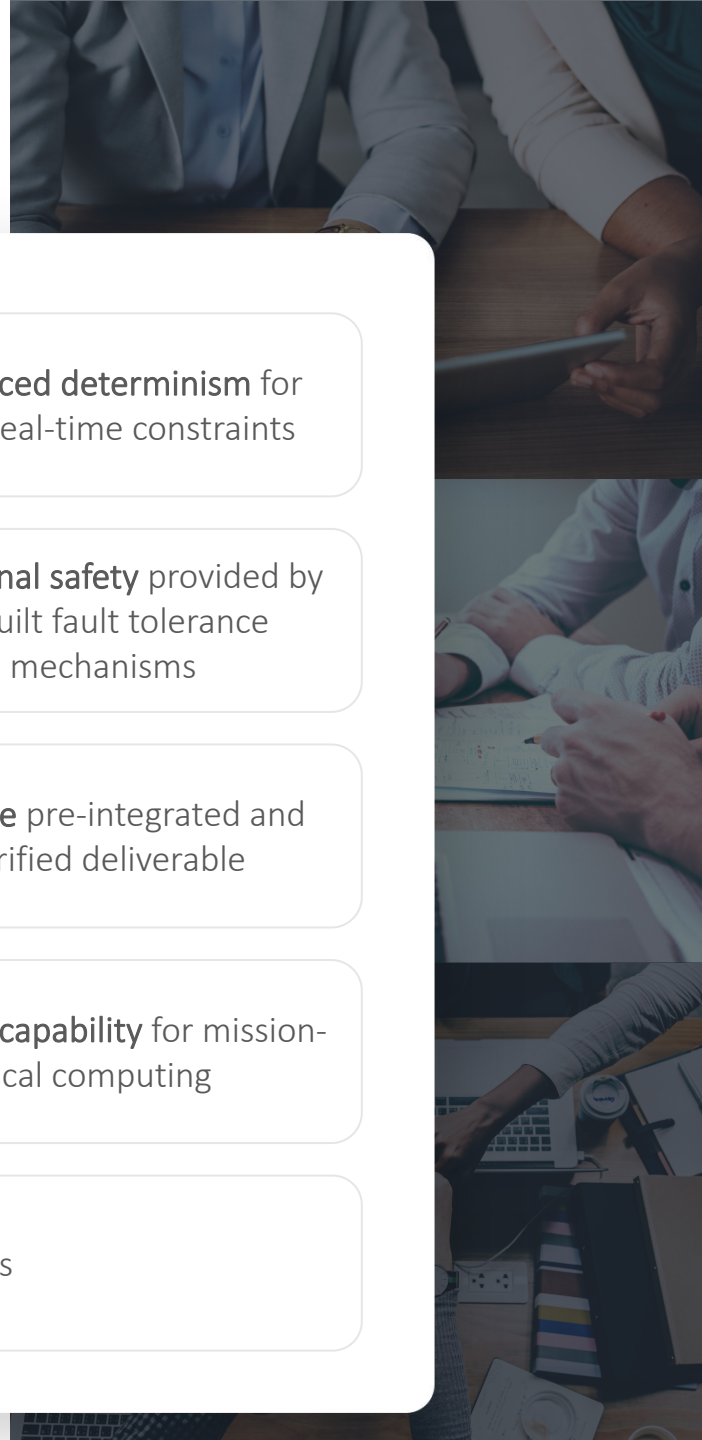
SiFive

7 series Core IP:

The **highest performance** commercial **RISC-V** processor IP



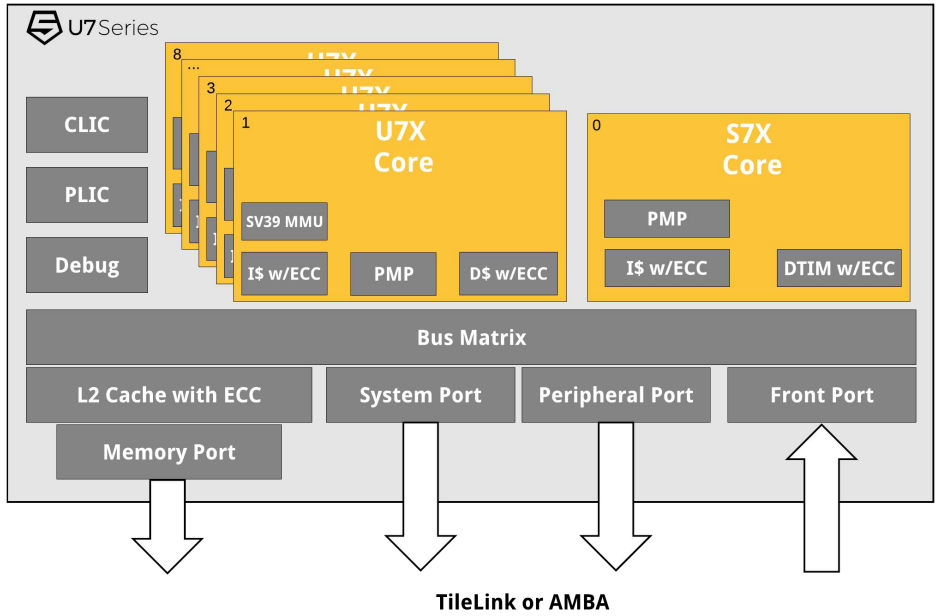
SiFive 7 Series
Embedded Intelligence Everywhere



Scalable throughput provided by **8+1** cores per cluster

Extensible design via custom instructions

Configurable memory architecture for application specific tuning



Enhanced determinism for hard real-time constraints

Functional safety provided by in-built fault tolerance mechanisms

A **single** pre-integrated and verified deliverable

Tightly integrated memory for low latency access

64-bit addressability for real time latency sensitive applications

Mixed-precision arithmetic for efficient compute of ML workloads

Cache lock capability for mission-critical computing

In-cluster coherent heterogenous combination of real-time and application processors

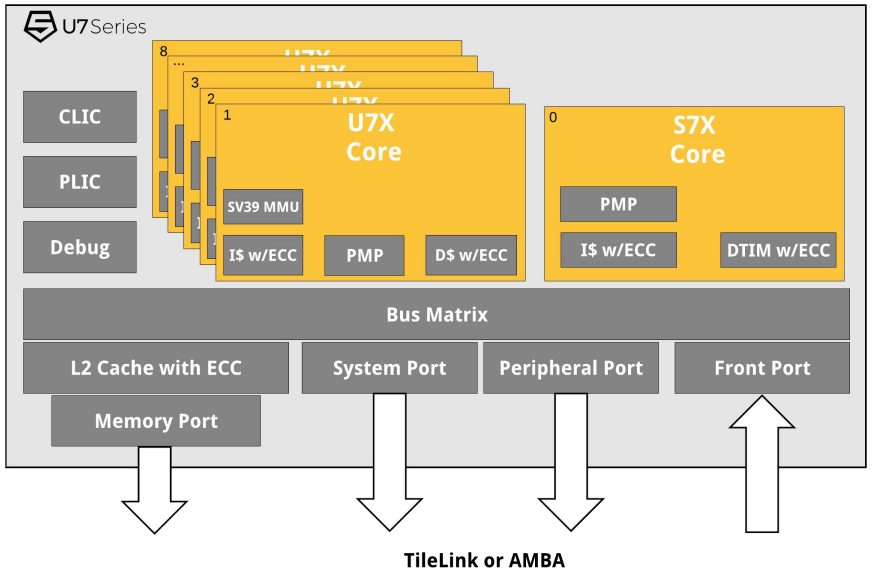
7 Series Core IP

Embedded Intelligence Everywhere

Scalable throughput provided by 8+1 cores per cluster

Extensible design via custom instructions

Configurable memory architecture for app specific tuning



Enhanced determinism for hard real-time constraints

Functional safety using built-in fault tolerant mechanisms

A **single** pre-integrated and verified deliverable

Tightly integrated memory for low latency access

64-bit addressability for real time latency sensitive applications

Mixed-precision arithmetic for efficient compute of ML workloads

Cache lock capability for mission-critical computing

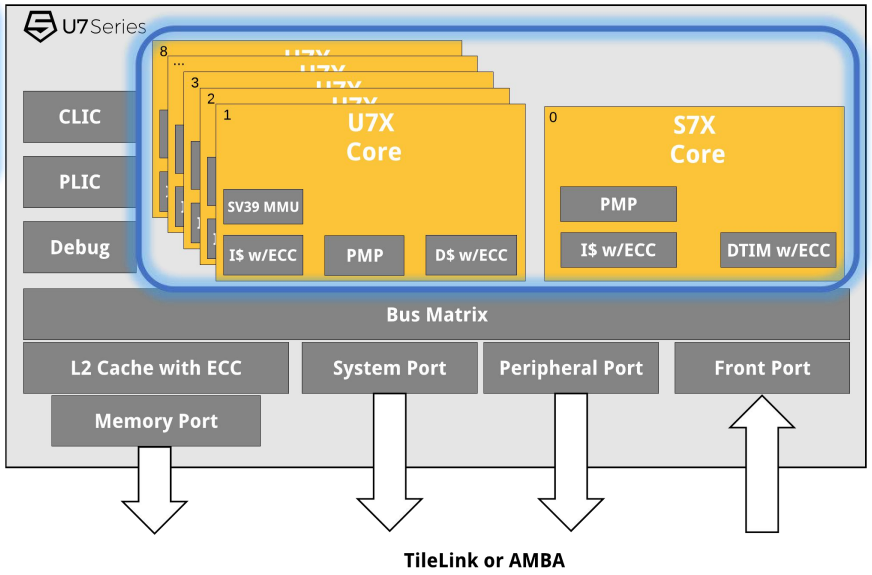
In-cluster coherent heterogenous combination of real-time and application processors

Storage

App + Real-Time Processors - Coherent in-cluster combinations

Storage, ML, Cryptography specific **custom instructions**

Configurable memory architecture for app specific tuning



Enhanced determinism for hard real-time constraints

Data Integrity using built-in fault tolerant mechanisms

Compute Acceleration Tightly coupled coherent accelerators or vector extensions

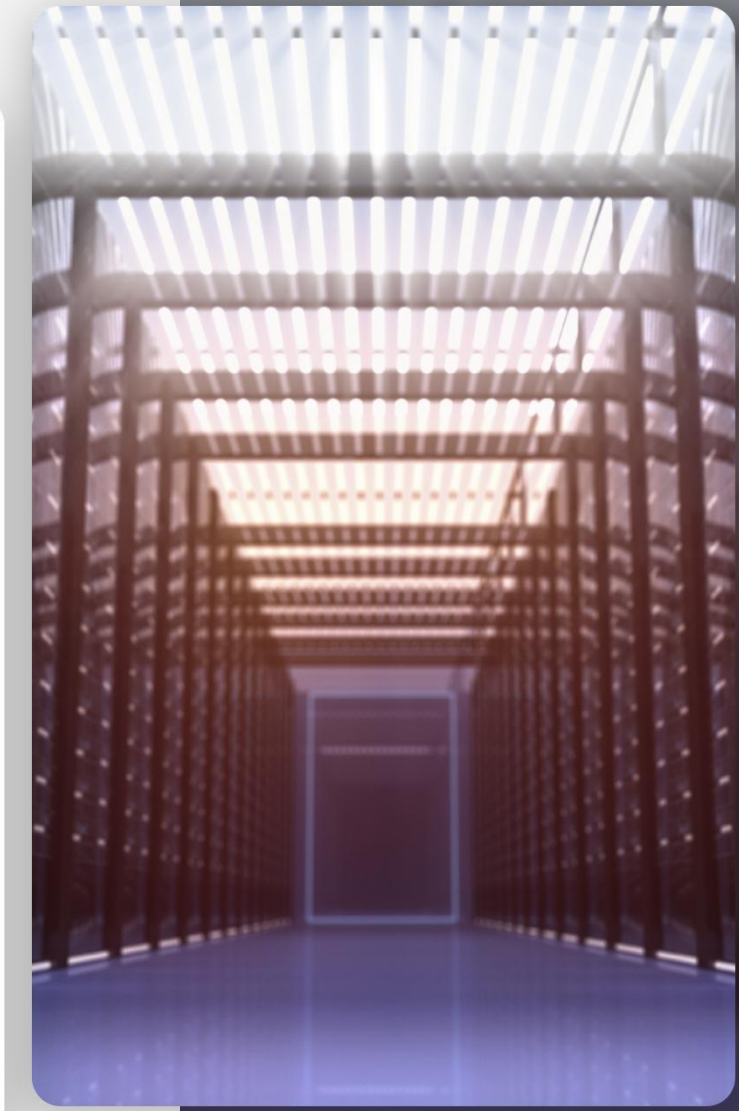
Tightly integrated memory for low latency access

64-bit addressability for BIG DATA applications

Optional FPU Optimize compute area to application need

Cache lock capability for mission-critical computing

In-cluster coherent heterogenous combination of real-time and application processors

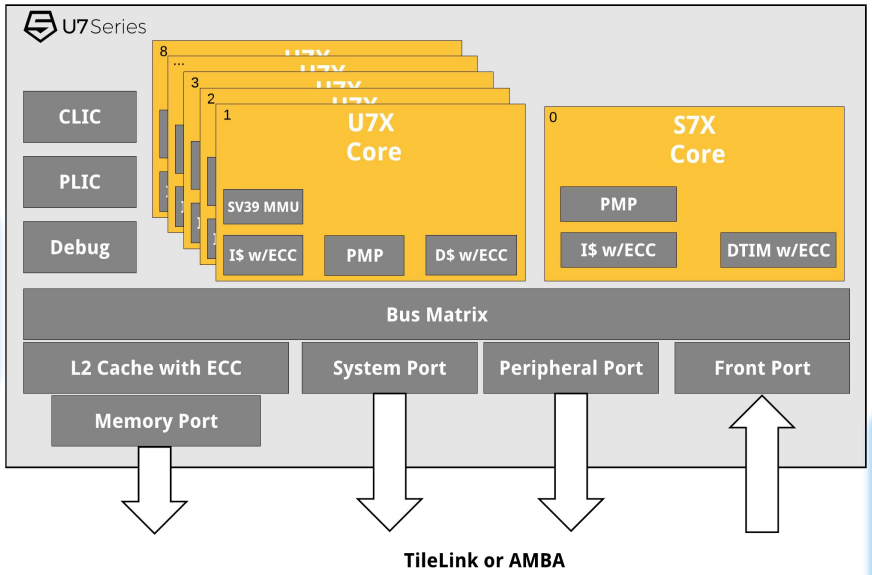


Storage

App + Real-Time Processors - Coherent in-cluster combinations

Storage, ML, Cryptography specific **custom instructions**

Configurable memory architecture for app specific tuning



Enhanced determinism for hard real-time constraints

Data Integrity using built-in fault tolerant mechanisms

Compute Acceleration Tightly coupled coherent accelerators or vector extensions

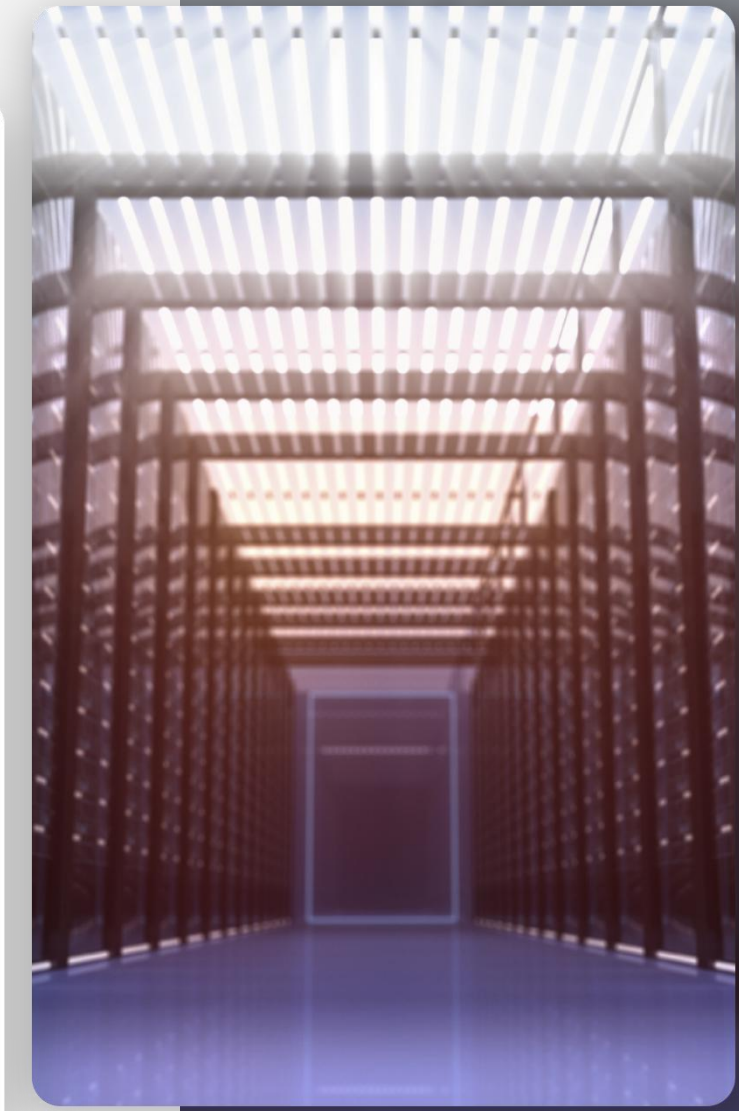
Tightly integrated memory for low latency access

64-bit addressability for BIG DATA applications

Optional FPU Optimize compute area to application need

Cache lock capability for mission-critical computing

In-cluster coherent heterogenous combination of real-time and application processors



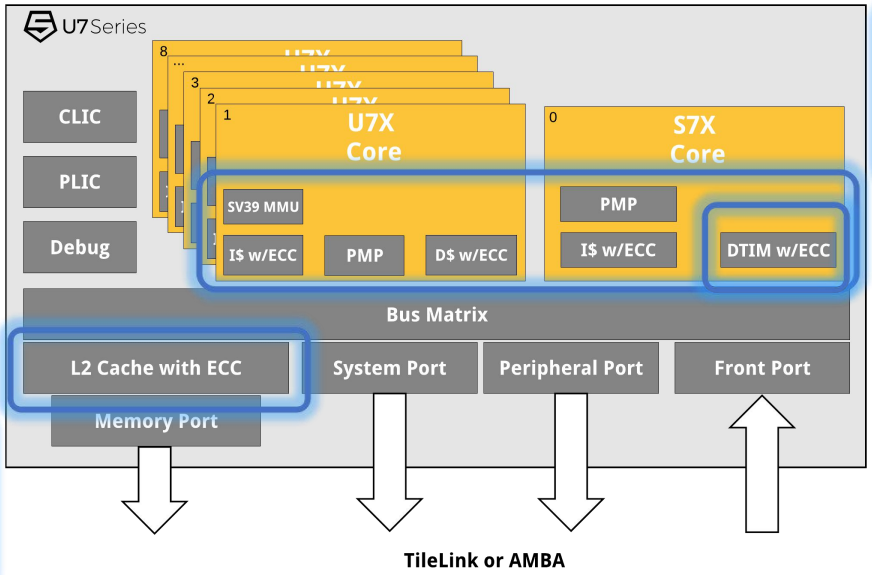
Storage

App + Real-Time Processors - Coherent in-cluster combinations

Storage, ML, Cryptography specific **custom instructions**

Configurable memory architecture for app specific tuning

Tightly integrated memory for low latency access



64-bit addressability for BIG DATA applications

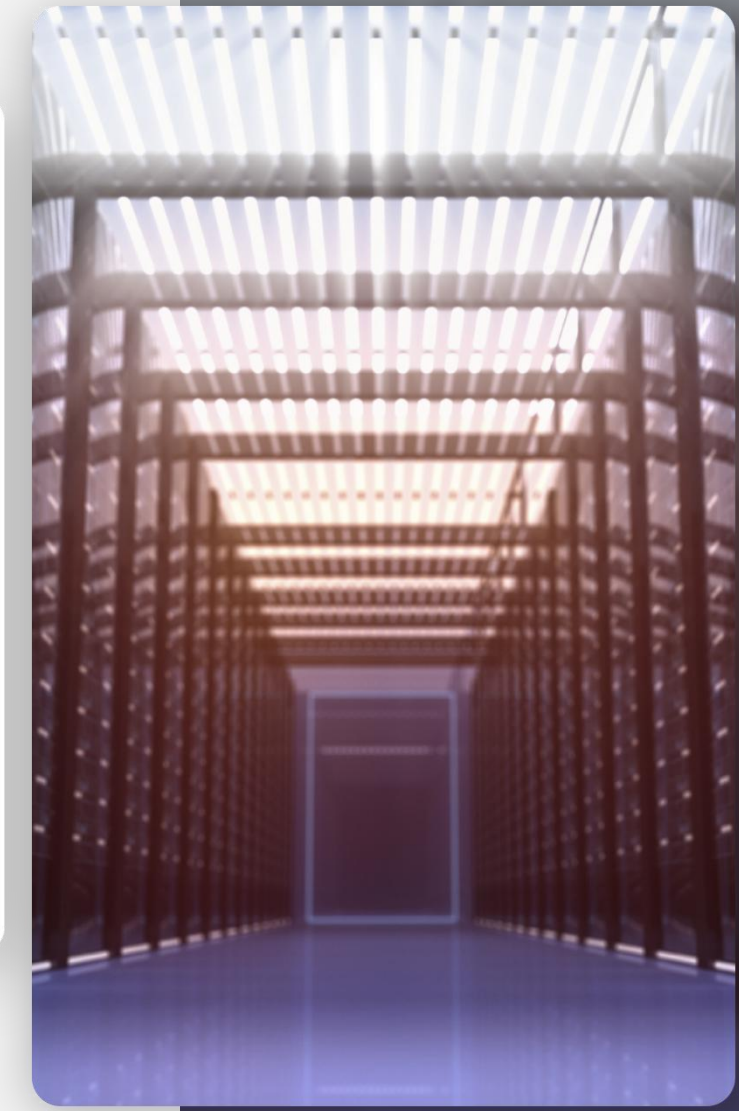
Optional FPU Optimize compute area to application need

Enhanced determinism for hard real-time constraints

Data Integrity using built-in fault tolerant mechanisms

Compute Acceleration Tightly coupled coherent accelerators or vector extensions

Cache lock capability for mission-critical computing

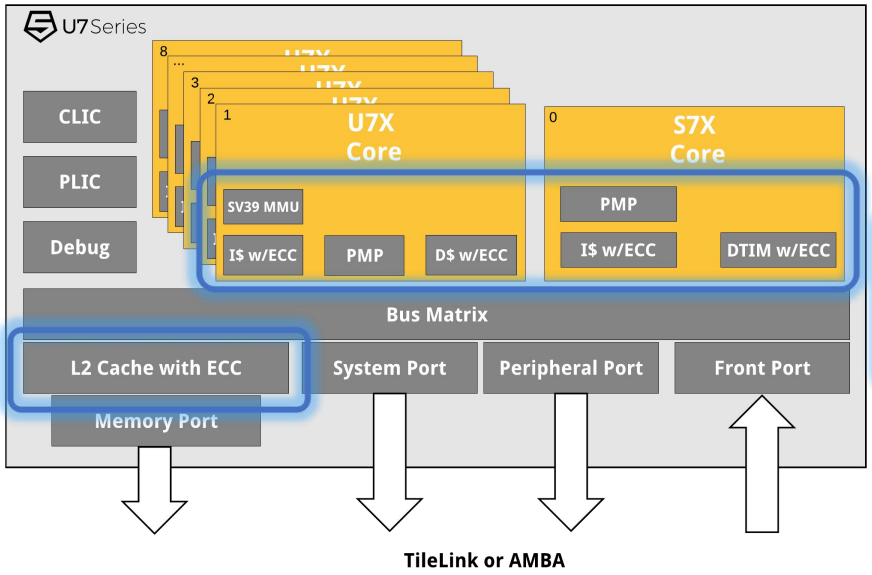


Storage

App + Real-Time Processors - Coherent in-cluster combinations

Storage, ML, Cryptography specific **custom instructions**

Configurable memory architecture for app specific tuning



Enhanced determinism for hard real-time constraints

Data Integrity using built-in fault tolerant mechanisms

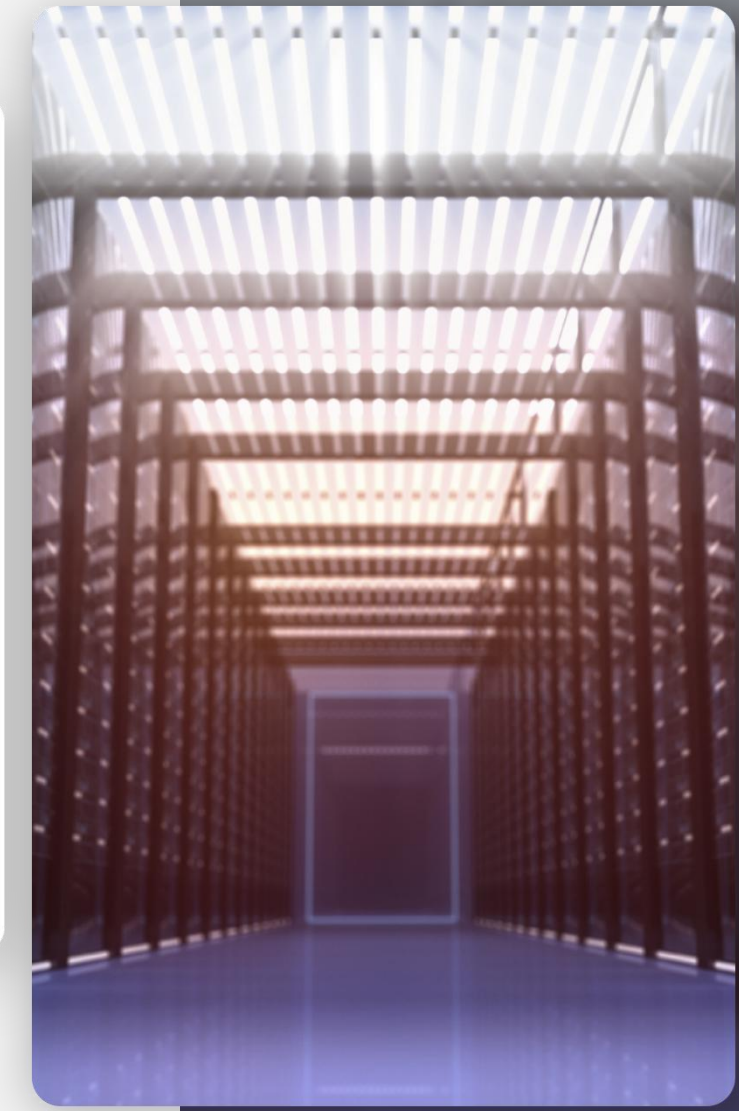
Compute Acceleration Tightly coupled coherent accelerators or vector extensions

Tightly integrated memory for low latency access

64-bit addressability for BIG DATA applications

Optional FPU Optimize compute area to application need

Cache lock capability for mission-critical computing



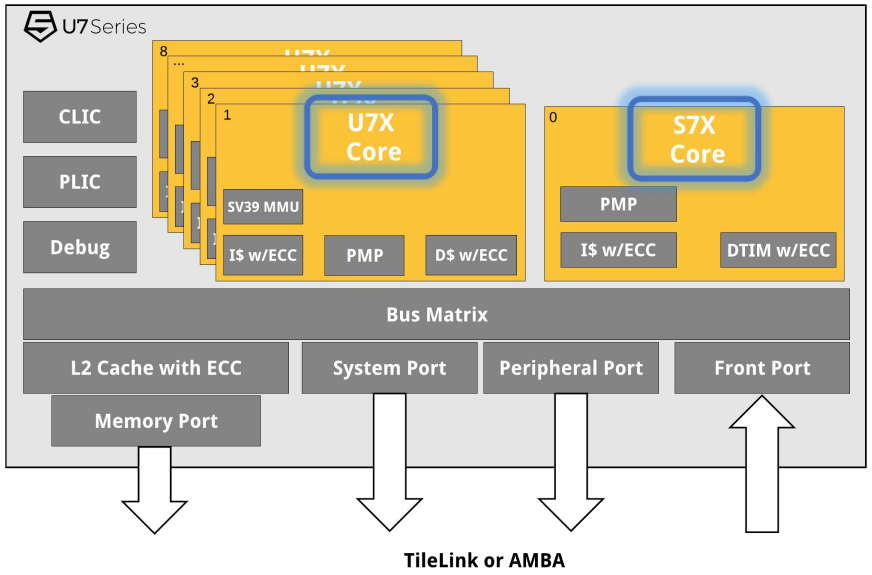
Storage

App + Real-Time Processors - Coherent in-cluster combinations

Storage, ML, Cryptography specific **custom instructions**

Configurable memory architecture for app specific tuning

Tightly integrated memory for low latency access



64-bit addressability for **BIG DATA** applications

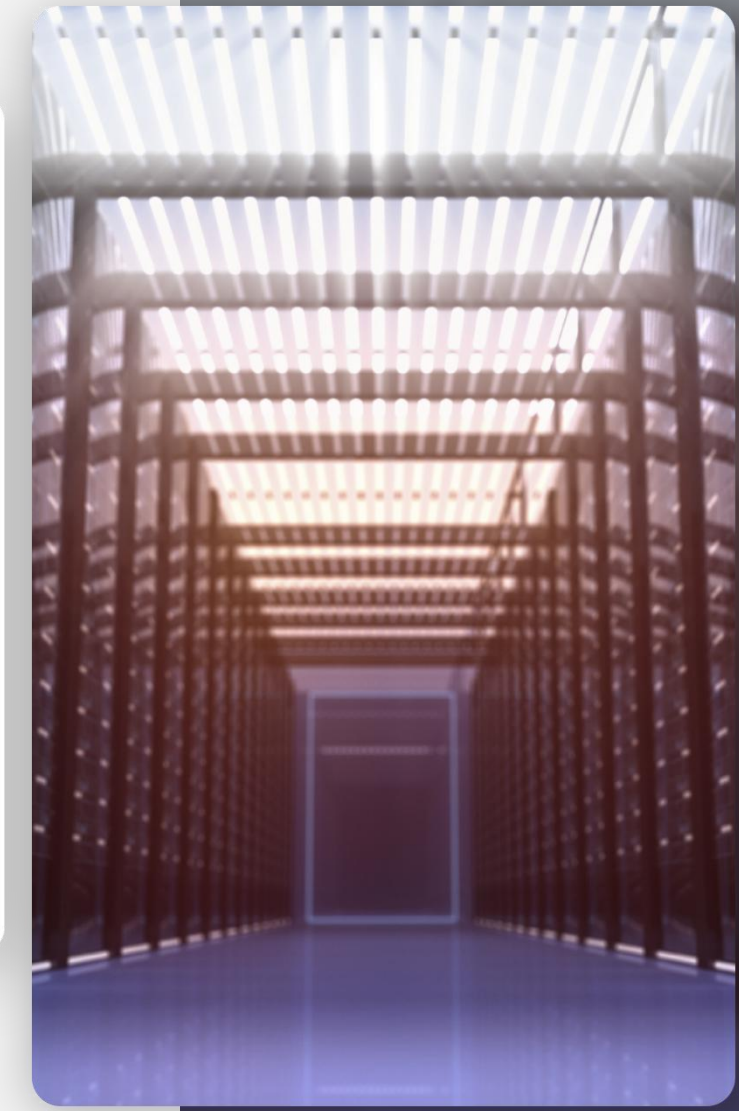
Optional FPU Optimize compute area to application need

Enhanced determinism for hard real-time constraints

Data Integrity using built-in fault tolerant mechanisms

Compute Acceleration Tightly coupled coherent accelerators or vector extensions

Cache lock capability for mission-critical computing

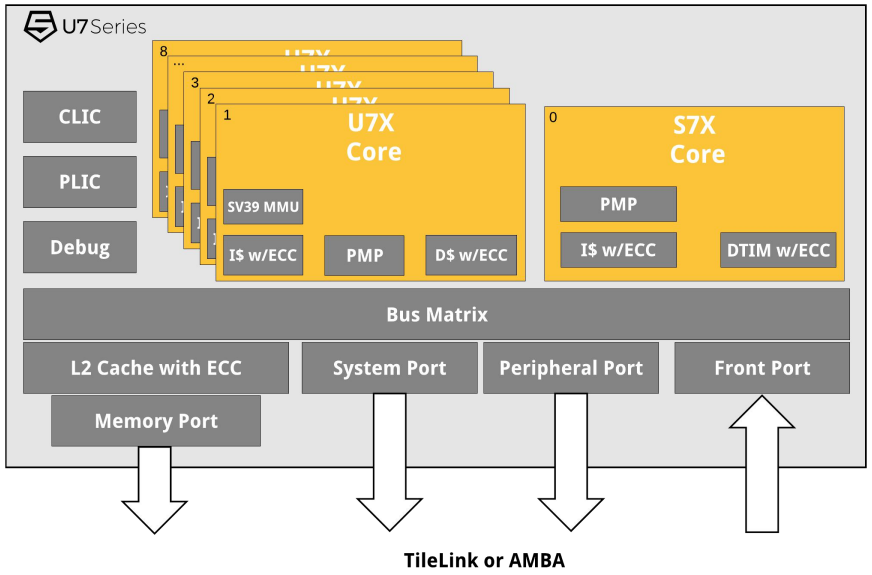


Storage

App + Real-Time Processors - Coherent in-cluster combinations

Storage, ML, Cryptography specific **custom instructions**

Configurable memory architecture for app specific tuning



Enhanced determinism for hard real-time constraints

Data Integrity using built-in fault tolerant mechanisms

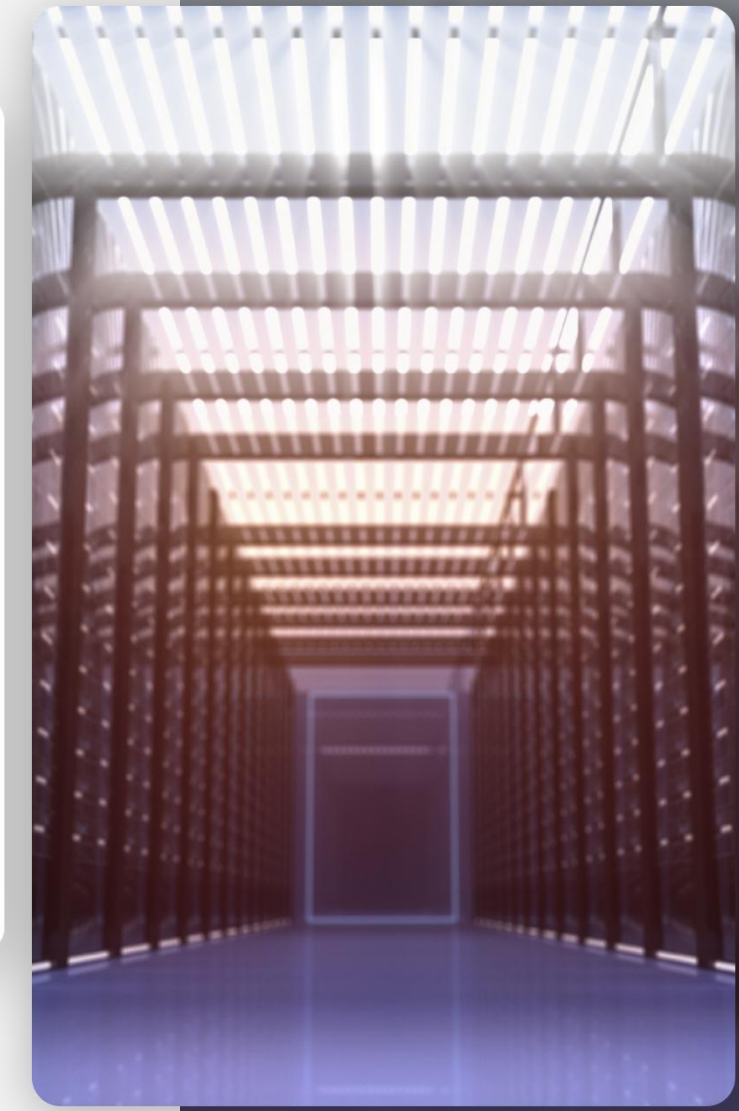
Compute Acceleration Tightly coupled coherent accelerators or vector extensions

Tightly integrated memory for low latency access

64-bit addressability for BIG DATA applications

Optional FPU Optimize compute area to application need

Cache lock capability for mission-critical computing



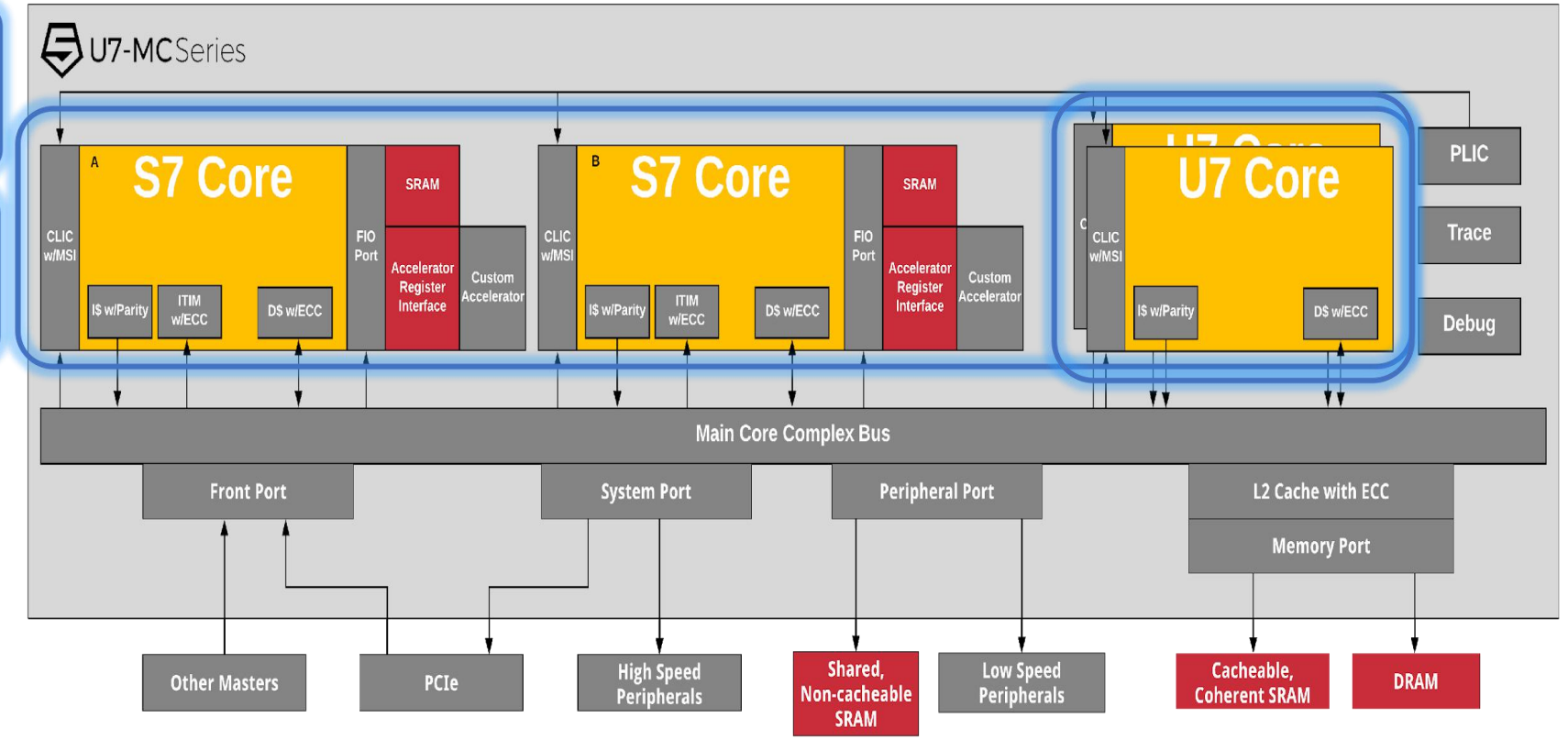
5G/Networking – Client and Enterprise

App + Real-Time Processors - Coherent in-cluster combinations

App processors High throughput 5G protocol stacks or SDN

Configurable memory architecture for optimizing QoS

Tightly integrated memory for 5G low latency response (1ms) and control routines



Hard RT capabilities Deterministic control of baseband processors

Front port DMA to RAM - network packet processing topologies

Compute Acceleration Tightly coupled coherent accelerators or vector extensions

64-bit addressability for large network address maps

Data Integrity for Enterprise systems using built-in fault tolerant mechanisms

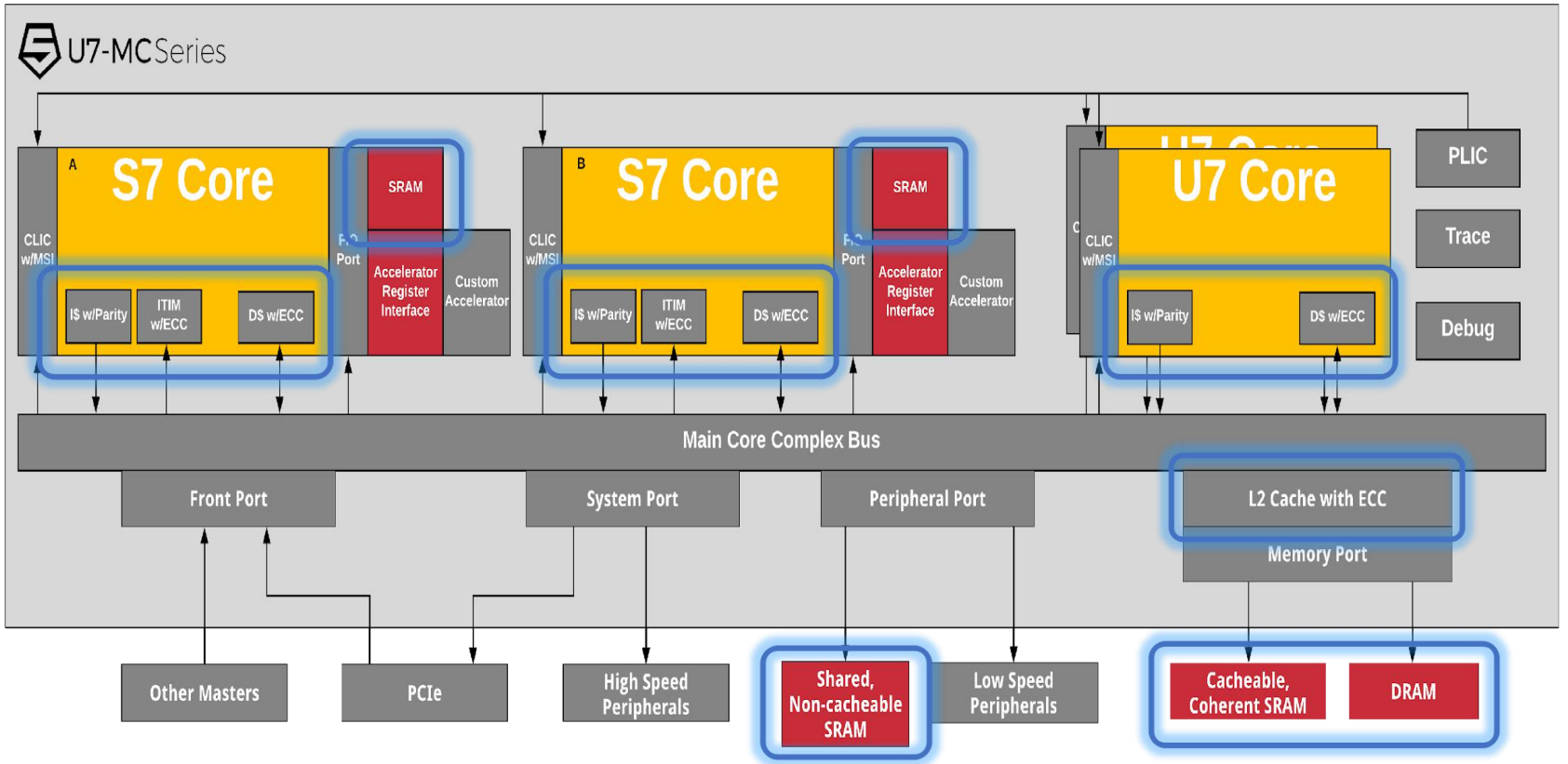
5G/Networking – Client and Enterprise

App + Real-Time Processors - Coherent in-cluster combinations

App processors High throughput 5G protocol stacks or SDN

Configurable memory architecture for optimizing QoS

Tightly integrated memory for 5G low latency response (1ms) and control routines



Hard RT capabilities Deterministic control of baseband processors

Front port DMA to RAM - network packet processing topologies

Compute Acceleration Tightly coupled coherent accelerators or vector extensions

64-bit addressability for large network address maps

Data Integrity for Enterprise systems using built-in fault tolerant mechanisms

5G/Networking – Client and Enterprise

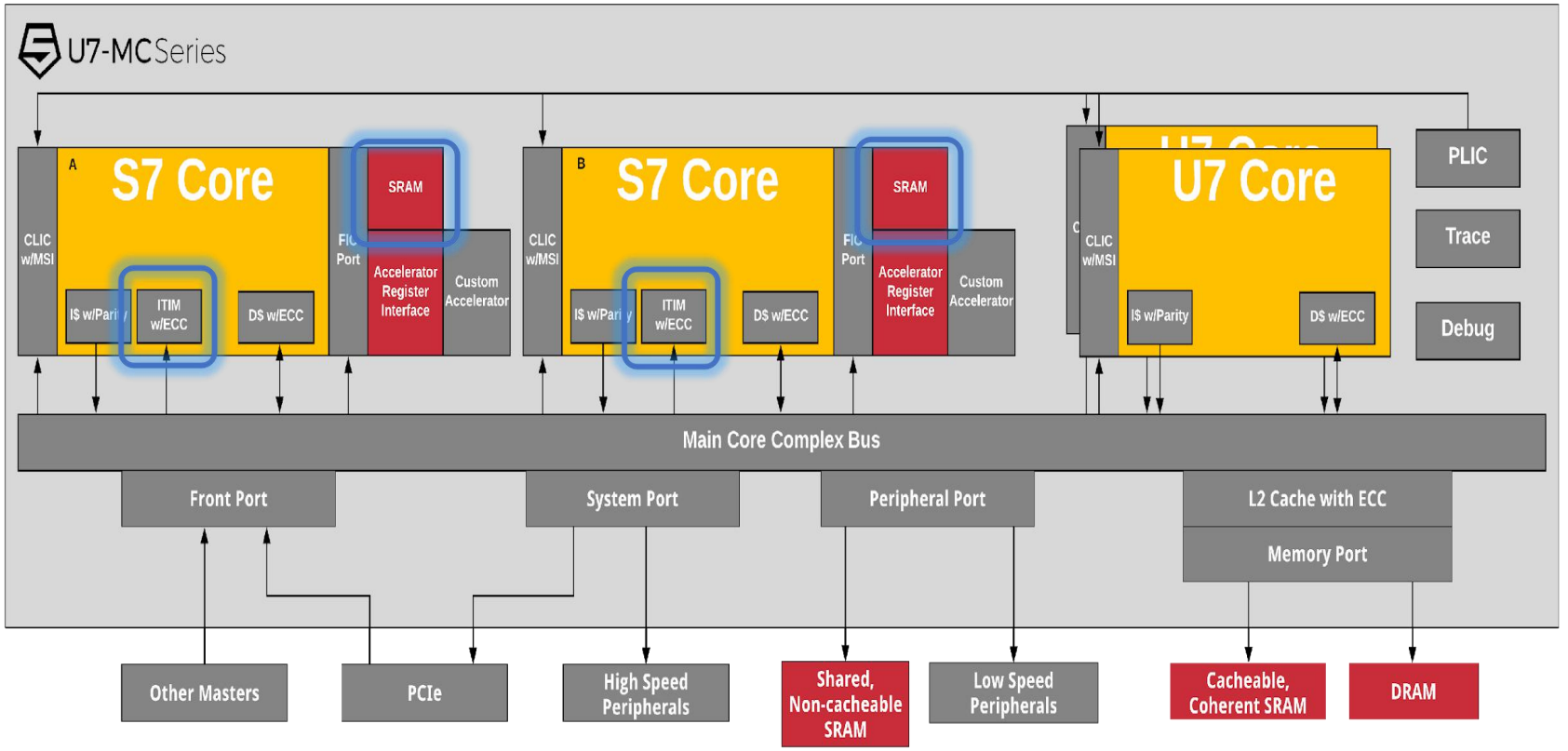
App + Real-Time Processors - Coherent in-cluster combinations

App processors High throughput 5G protocol stacks or SDN

Configurable memory architecture for optimizing QoS

Tightly integrated memory for 5G low latency response (1ms) and control routines

Hard RT capabilities Deterministic control of baseband processors



Front port DMA to RAM - network packet processing topologies

Compute Acceleration Tightly coupled coherent accelerators or vector extensions

64-bit addressability for large network address maps

Data Integrity for Enterprise systems using built-in fault tolerant mechanisms

5G/Networking – Client and Enterprise

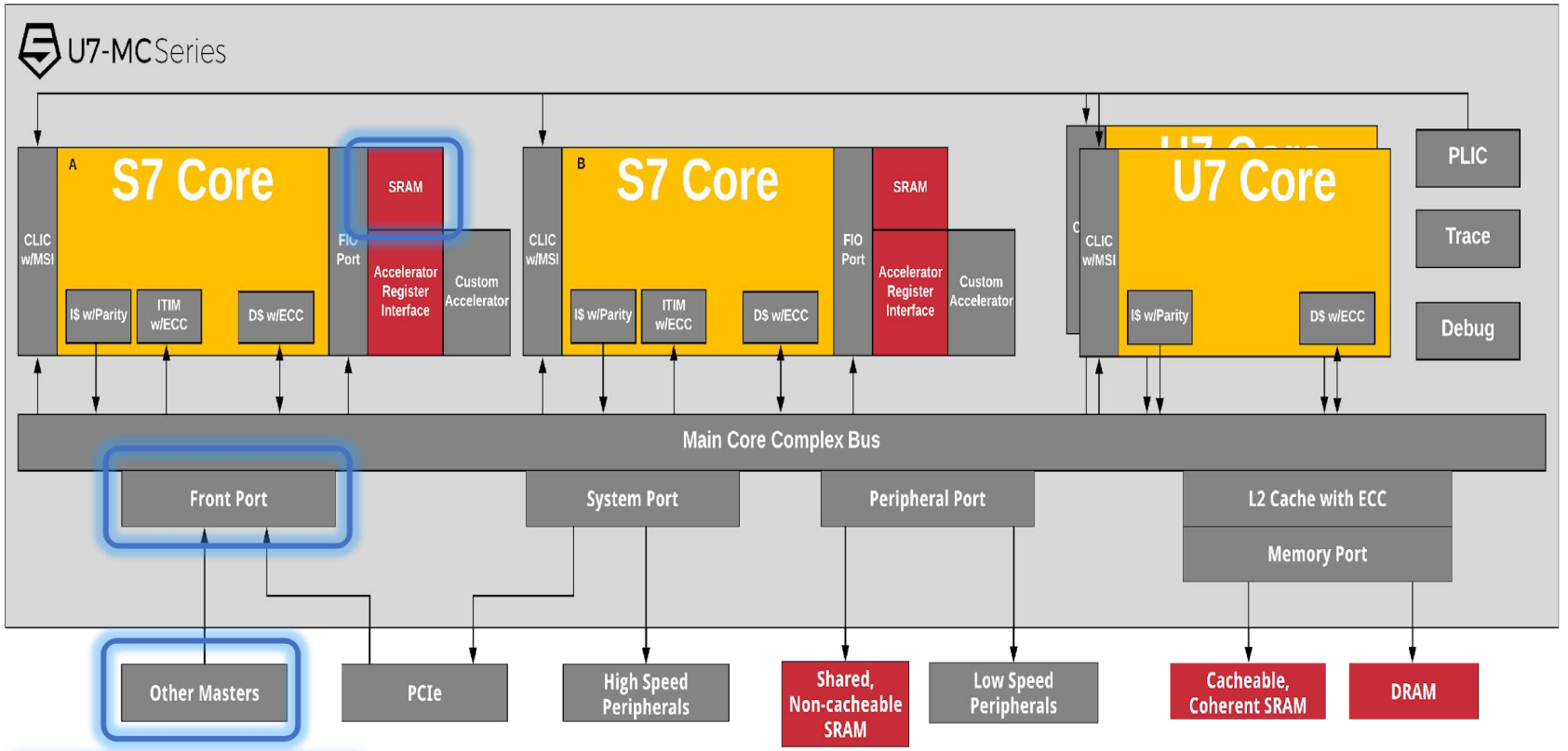
App + Real-Time Processors - Coherent in-cluster combinations

App processors High throughput 5G protocol stacks or SDN

Configurable memory architecture for optimizing QoS

Tightly integrated memory for 5G low latency response (1ms) and control routines

Hard RT capabilities Deterministic control of baseband processors



Front port DMA to RAM - network packet processing topologies

Compute Acceleration Tightly coupled coherent accelerators or vector extensions

64-bit addressability for large network address maps

Data Integrity for Enterprise systems using built-in fault tolerant mechanisms

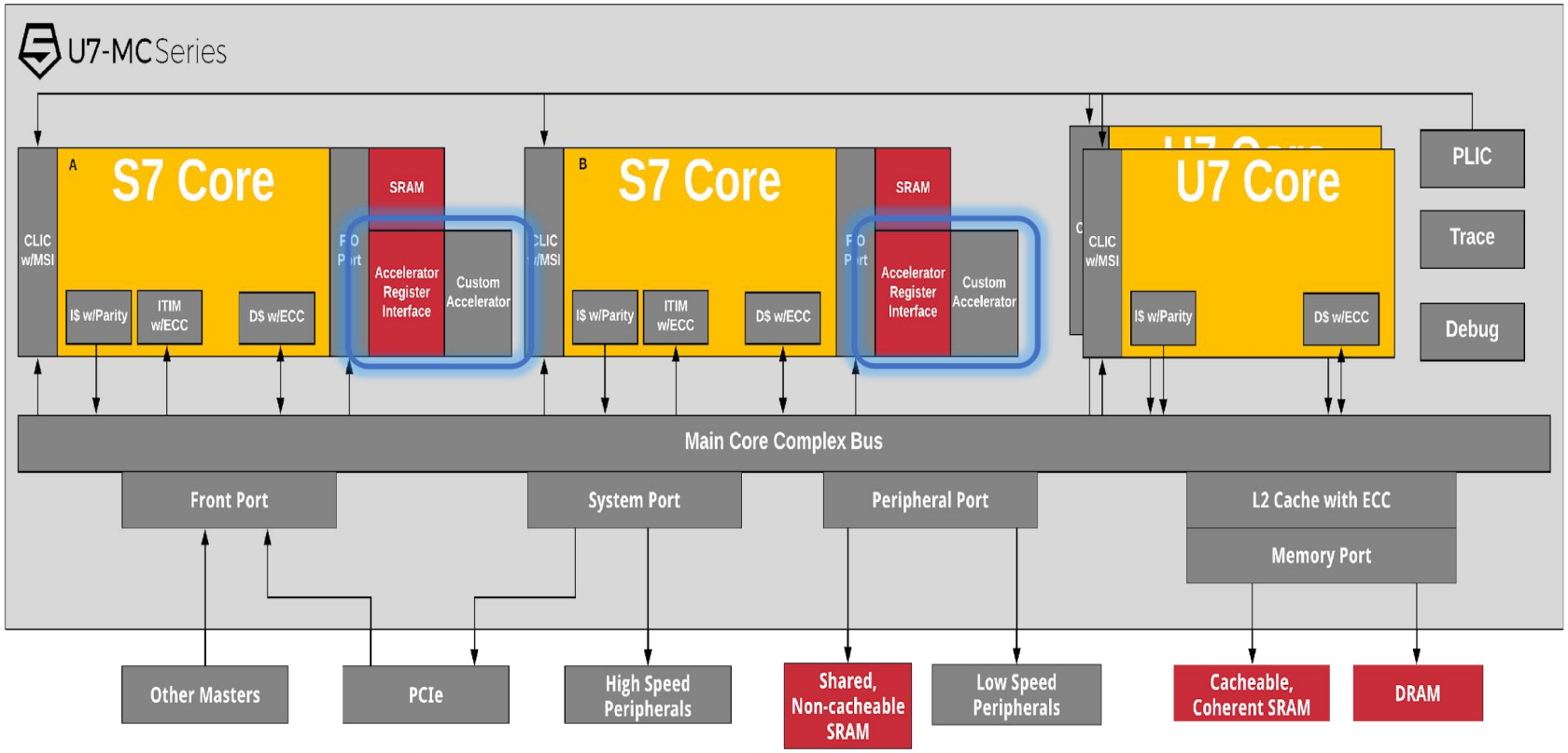
5G/Networking – Client and Enterprise

App + Real-Time Processors - Coherent in-cluster combinations

App processors High throughput 5G protocol stacks or SDN

Configurable memory architecture for optimizing QoS

Tightly integrated memory for 5G low latency response (1ms) and control routines



Hard RT capabilities Deterministic control of baseband processors

Front port DMA to RAM - network packet processing topologies

Compute Acceleration Tightly coupled coherent accelerators or vector extensions

64-bit addressability for large network address maps

Data Integrity for Enterprise systems using built-in fault tolerant mechanisms

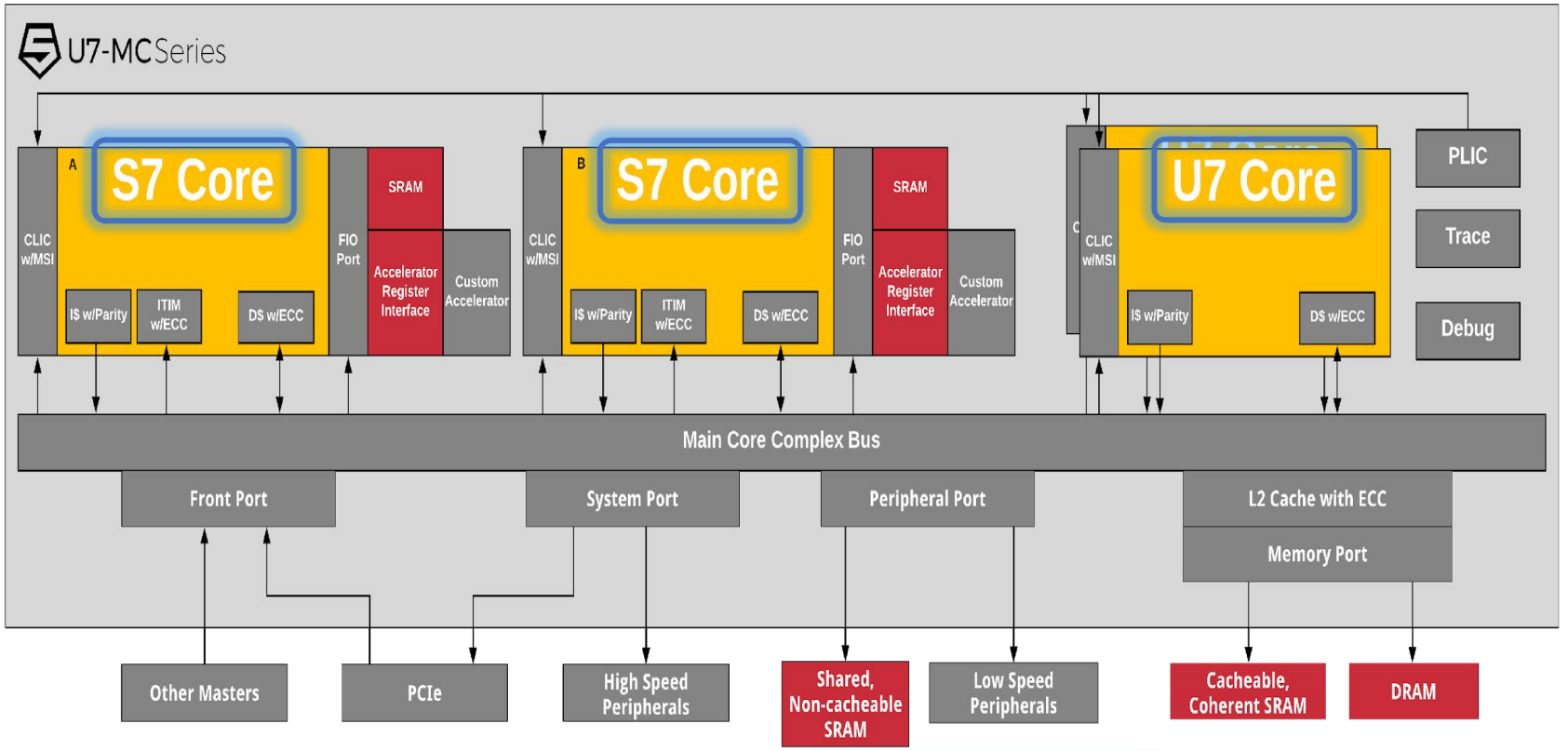
5G/Networking – Client and Enterprise

App + Real-Time Processors - Coherent in-cluster combinations

App processors High throughput 5G protocol stacks or SDN

Configurable memory architecture for optimizing QoS

Tightly integrated memory for 5G low latency response and control routines



Hard RT capabilities Deterministic control of baseband processors

Front port DMA to RAM - network packet processing topologies

Compute Acceleration Tightly coupled coherent accelerators or vector extensions

64-bit addressability for large network address maps

Data Integrity for Enterprise systems using built-in fault tolerant mechanisms

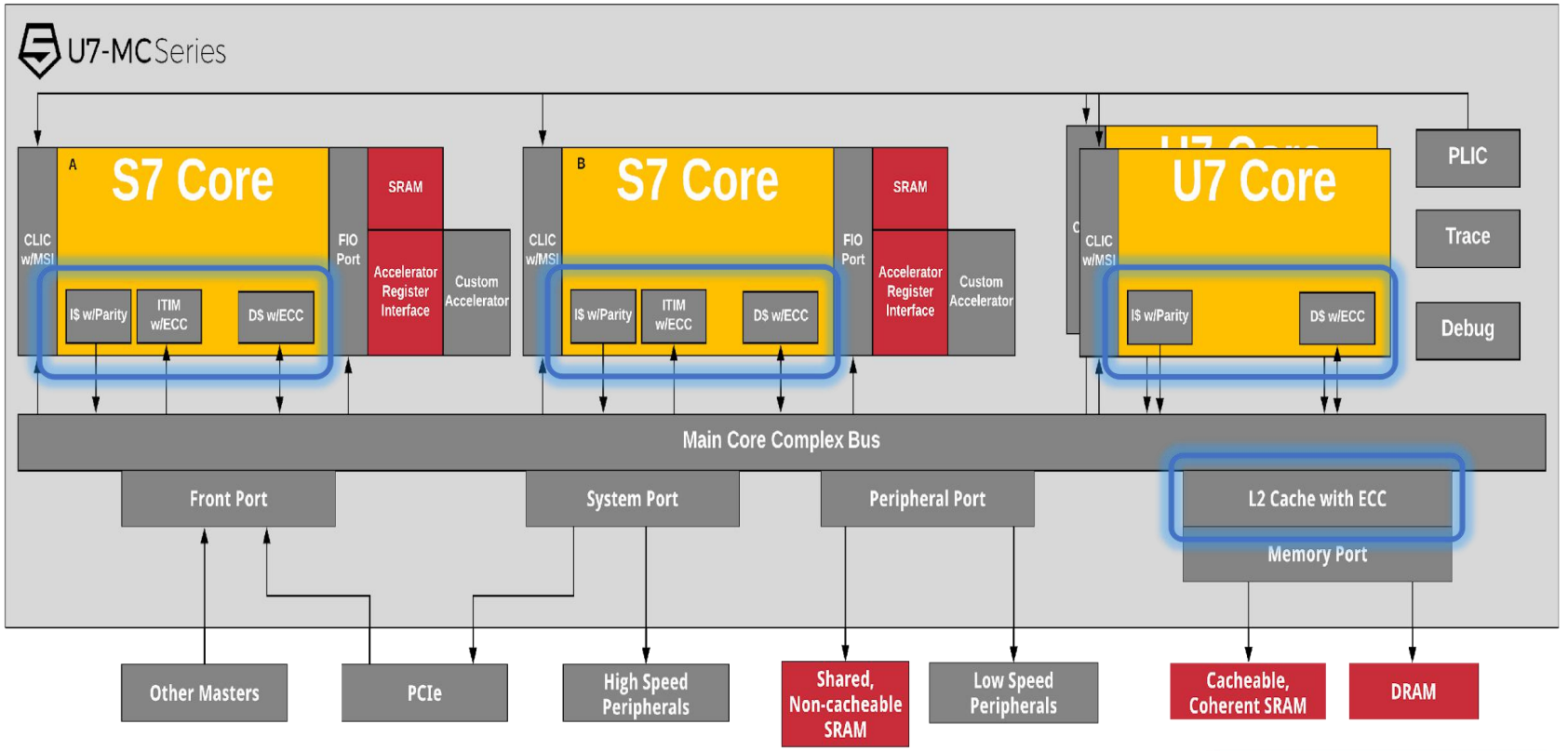
5G/Networking – Client and Enterprise

App + Real-Time Processors - Coherent in-cluster combinations

App processors High throughput 5G protocol stacks or SDN

Configurable memory architecture for optimizing QoS

Tightly integrated memory for 5G low latency response (1ms) and control routines



Hard RT capabilities Deterministic control of baseband processors

Front port DMA to RAM - network packet processing topologies

Compute Acceleration Tightly coupled coherent accelerators or vector extensions

64-bit addressability for large network address maps

Data Integrity for Enterprise systems using built-in fault tolerant mechanisms

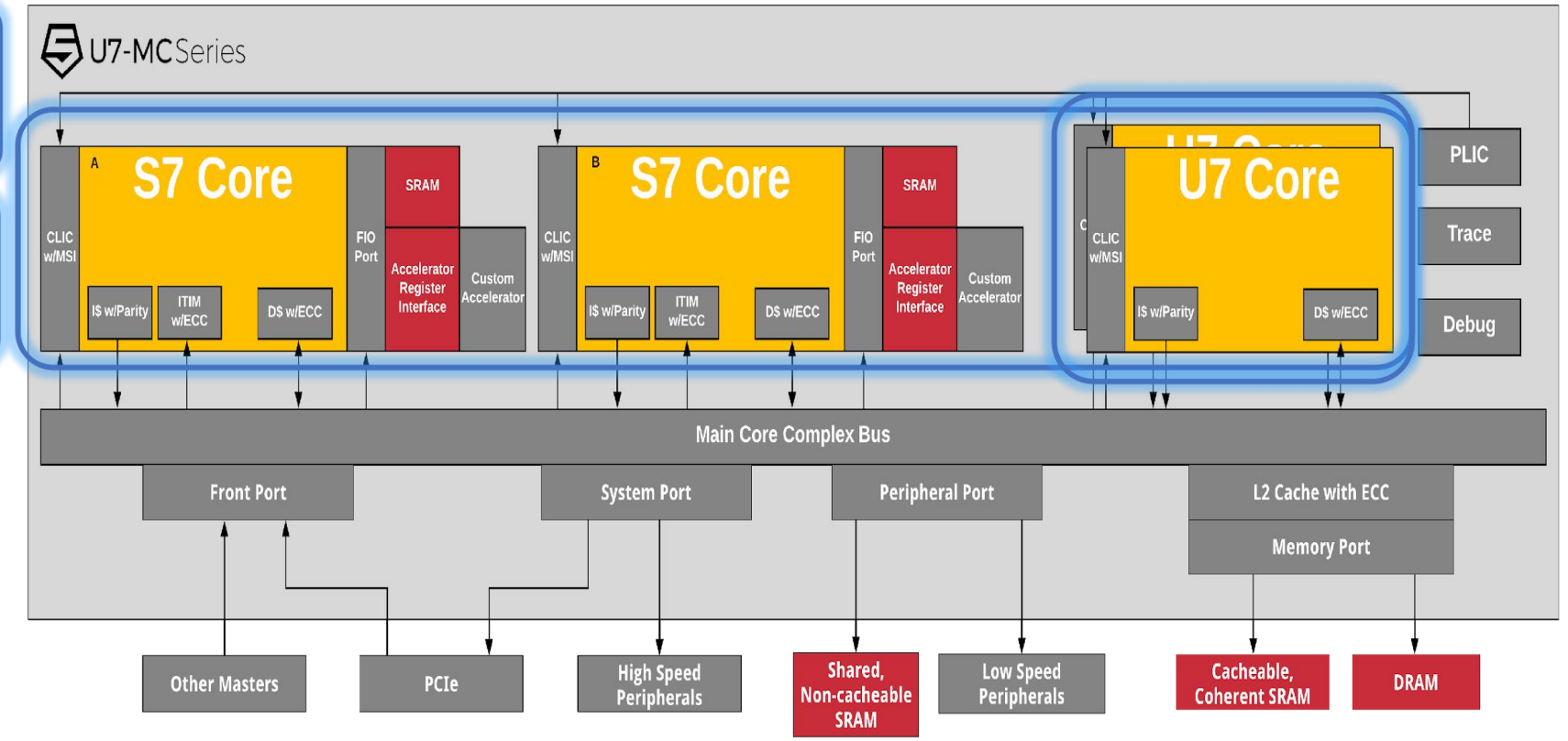
AR/VR/Sensor Fusion

App + Real-Time Processors - Coherent in-cluster combinations

App processors
Run high performance Linux and user apps

Simple caching hierarchy for ease of application optimization

Low Latency peripheral access

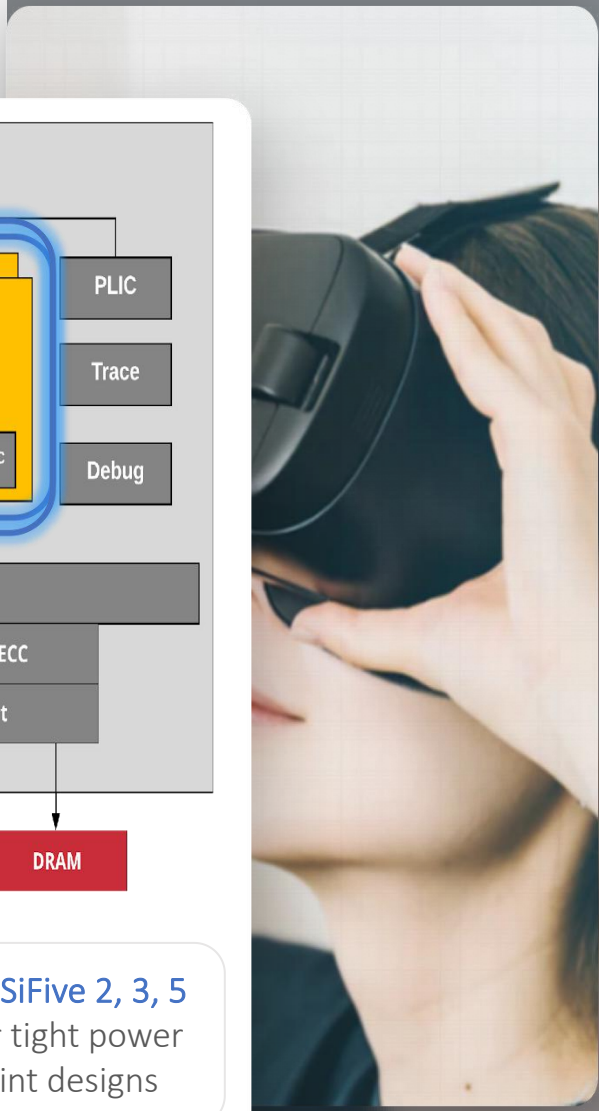


AR/VR/MR/CV Workloads Accelerators, vector extensions, SCIE

Mixed precision arithmetic for accelerating machine learning compute

64-bit addressability and scalar compute for complex graphics

Use with SiFive 2, 3, 5 series for tight power constraint designs



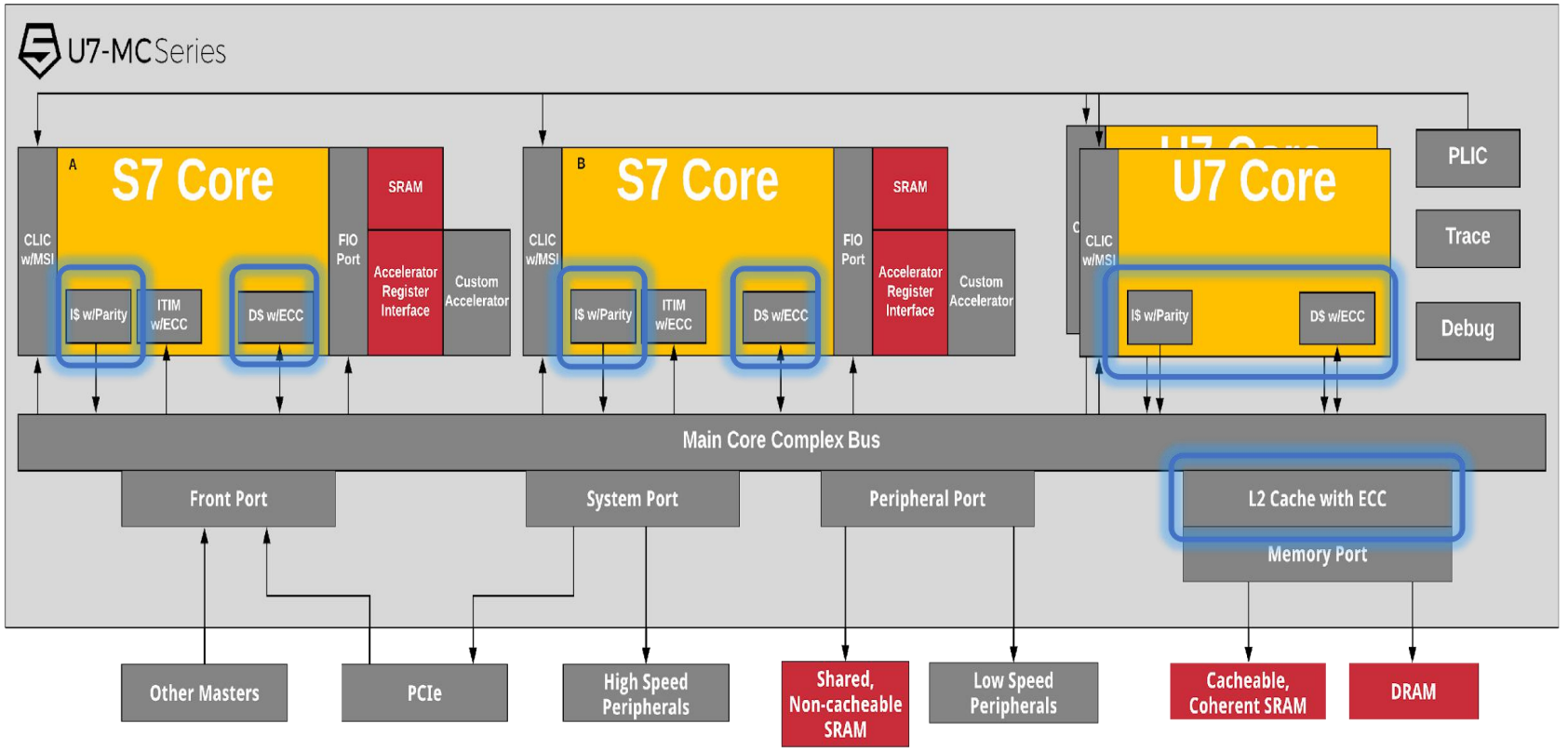
AR/VR/Sensor Fusion

App + Real-Time Processors - Coherent in-cluster combinations

App processors
Run high performance Linux and user apps

Simple caching hierarchy for ease of application optimization

Low Latency peripheral access

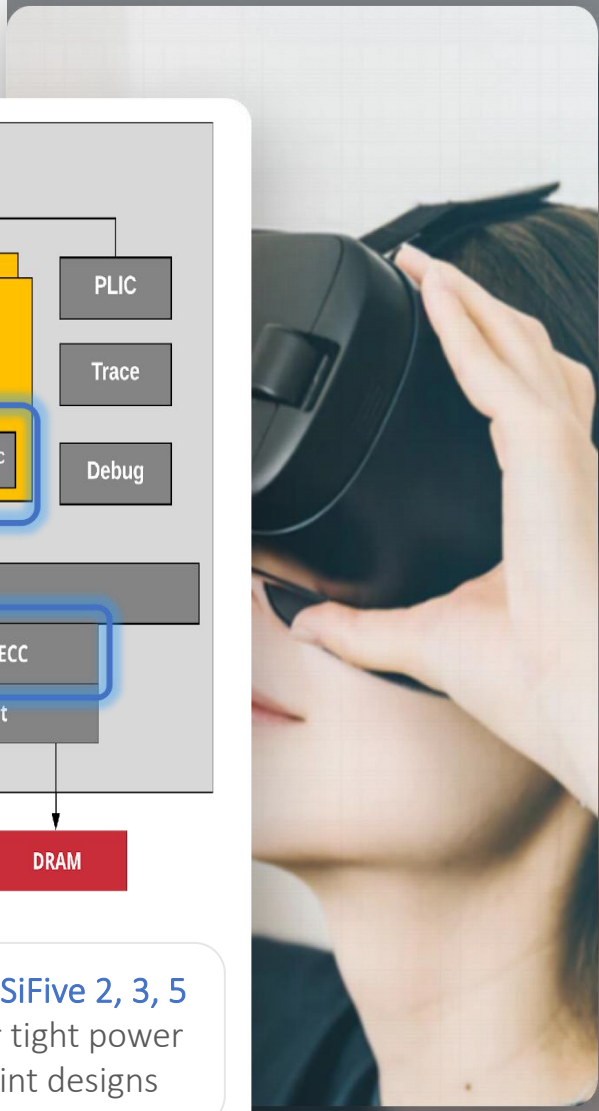


AR/VR/MR/CV Workloads Accelerators, vector extensions, SCIE

Mixed precision arithmetic for accelerating machine learning compute

64-bit addressability and scalar compute for complex graphics

Use with SiFive 2, 3, 5 series for tight power constraint designs



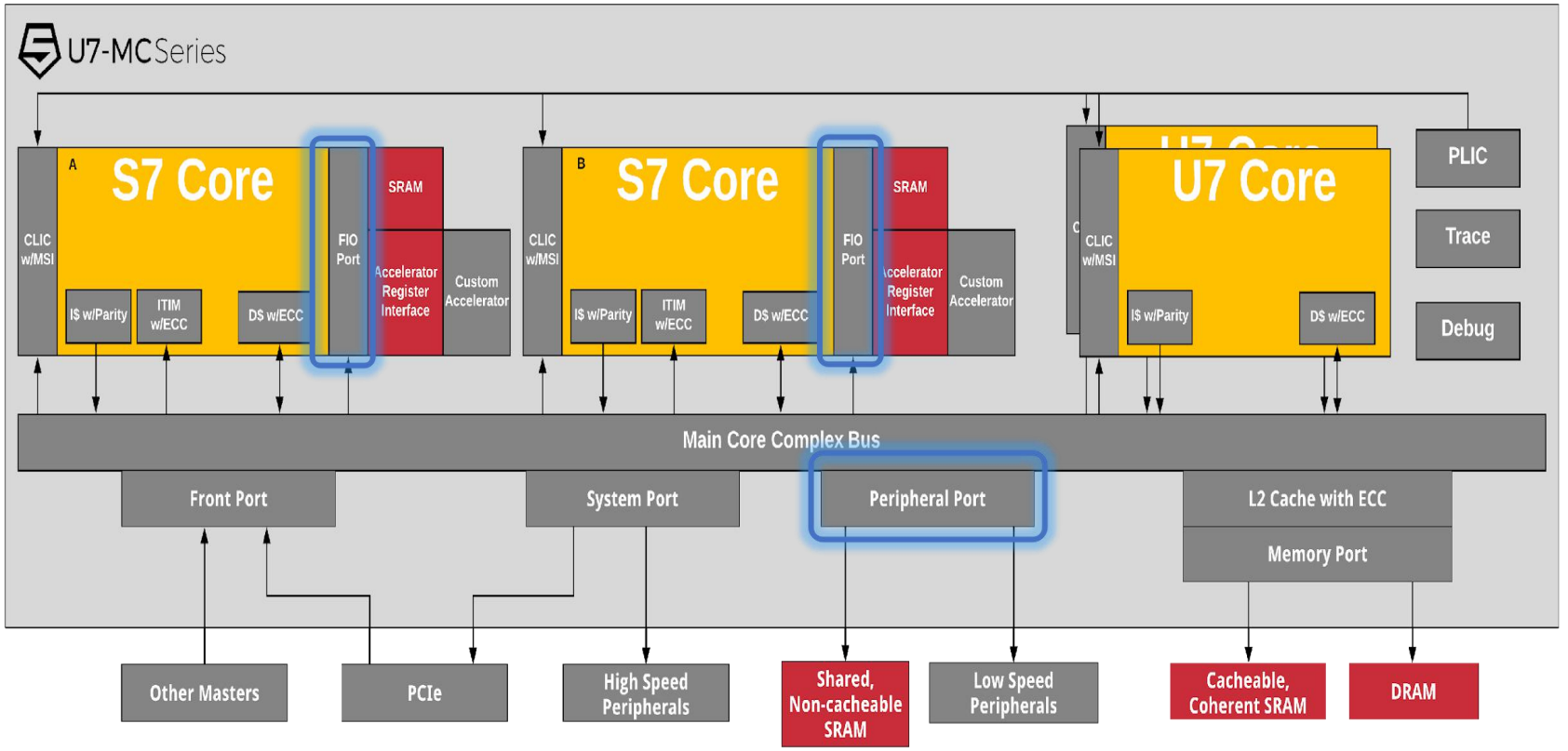
AR/VR/Sensor Fusion

App + Real-Time Processors - Coherent in-cluster combinations

App processors Run high performance Linux and user apps

Simple caching hierarchy for ease of application optimization

Low Latency peripheral access

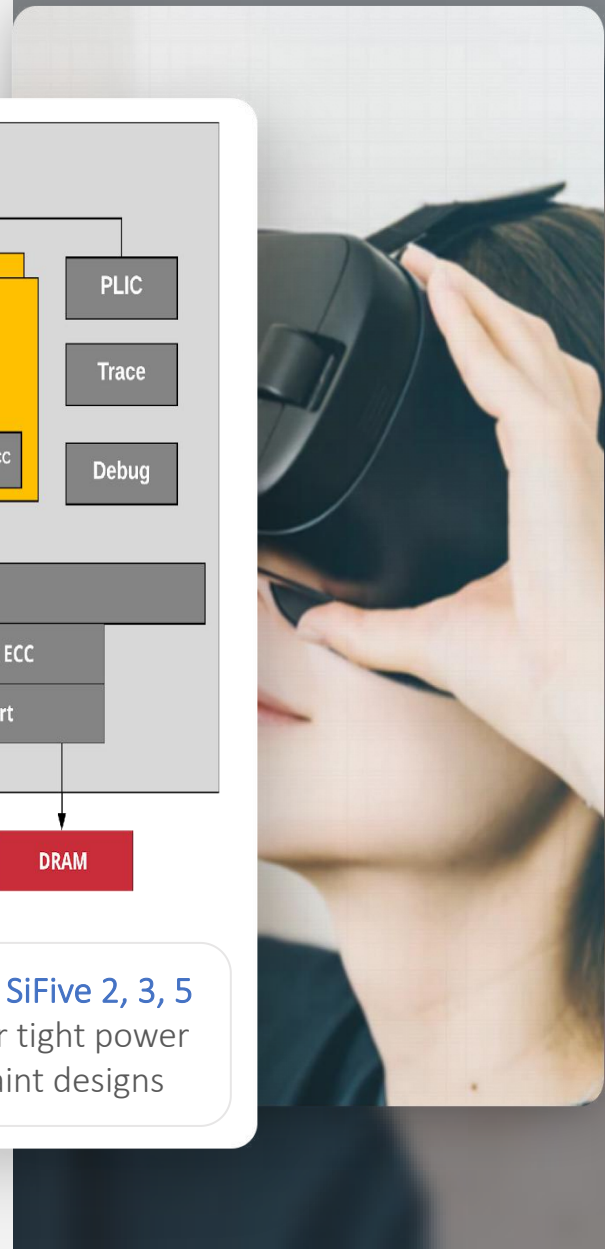


AR/VR/MR/CV Workloads Accelerators, vector extensions, SCIE

Mixed precision arithmetic for accelerating machine learning compute

64-bit addressability and scalar compute for complex graphics

Use with SiFive 2, 3, 5 series for tight power constraint designs



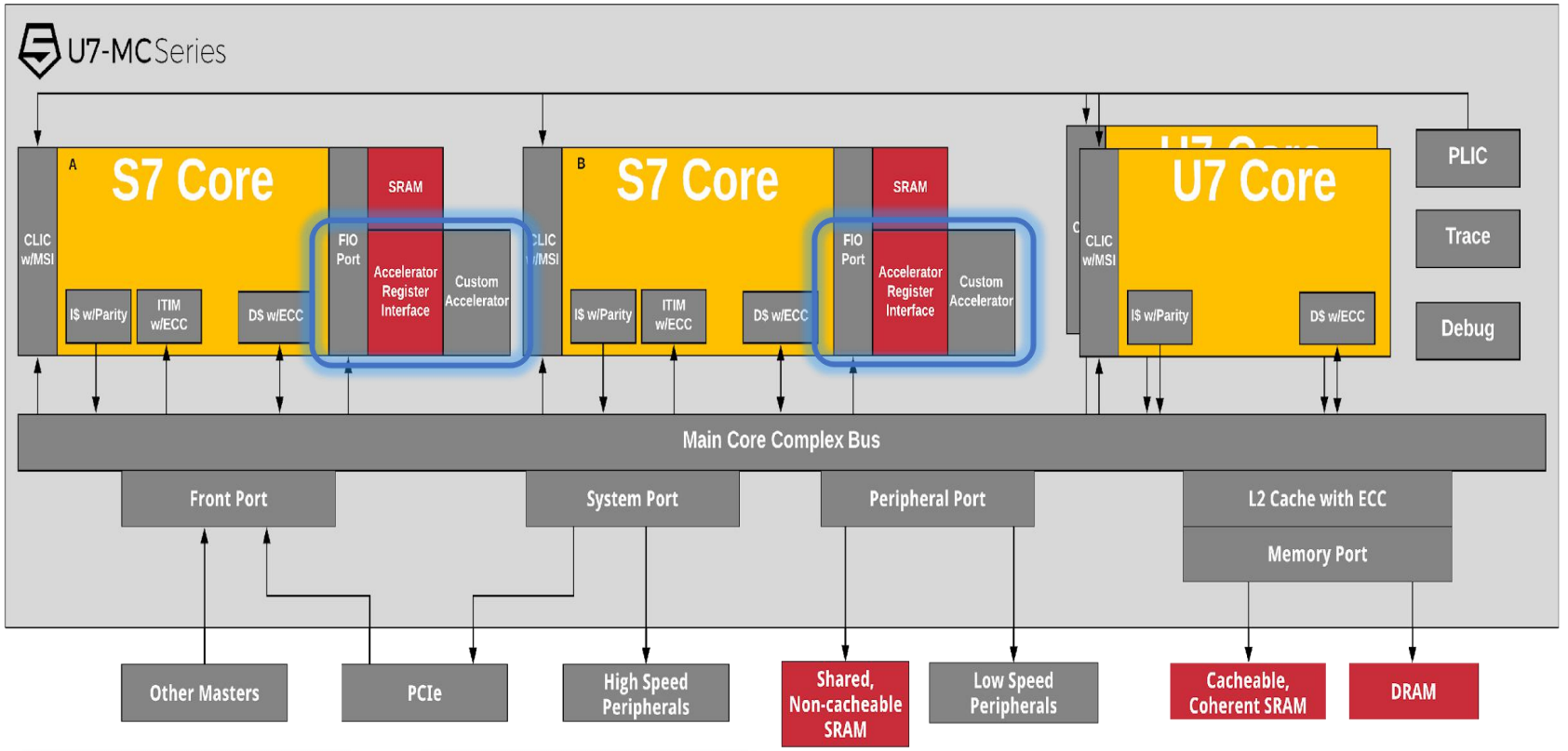
AR/VR/Sensor Fusion

App + Real-Time Processors - Coherent in-cluster combinations

App processors
Run high performance Linux and user apps

Simple caching hierarchy for ease of application optimization

Low Latency peripheral access

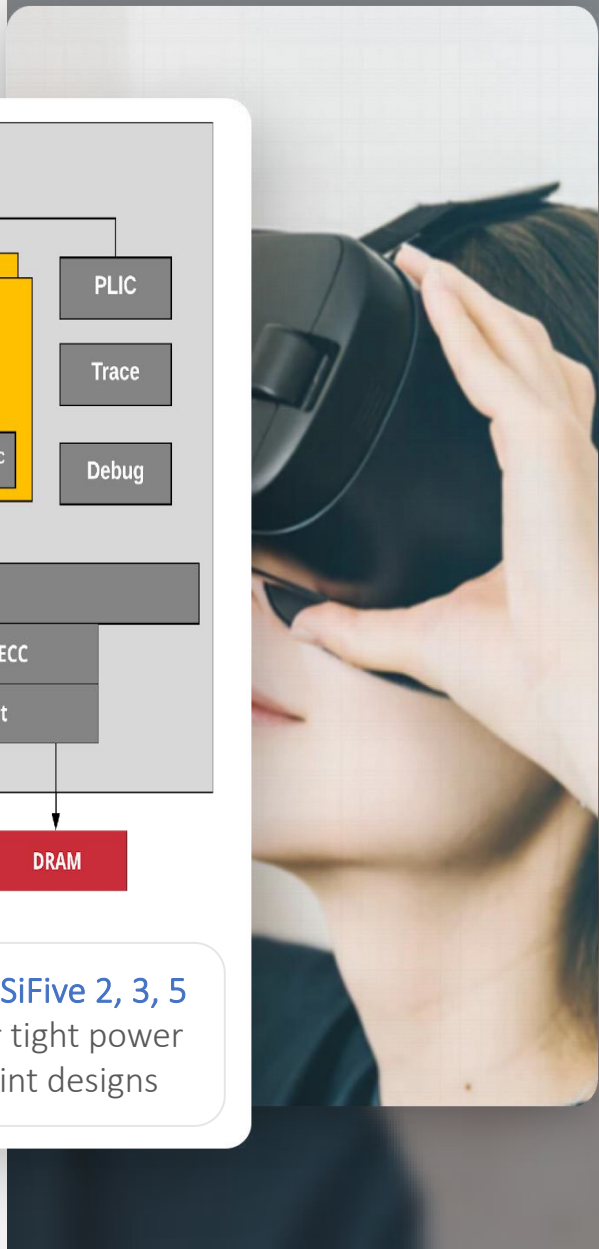


AR/VR/MR/CV Workloads Accelerators, vector extensions, SCIE

Mixed precision arithmetic for accelerating machine learning compute

64-bit addressability and scalar compute for complex graphics

Use with SiFive 2, 3, 5 series for tight power constraint designs



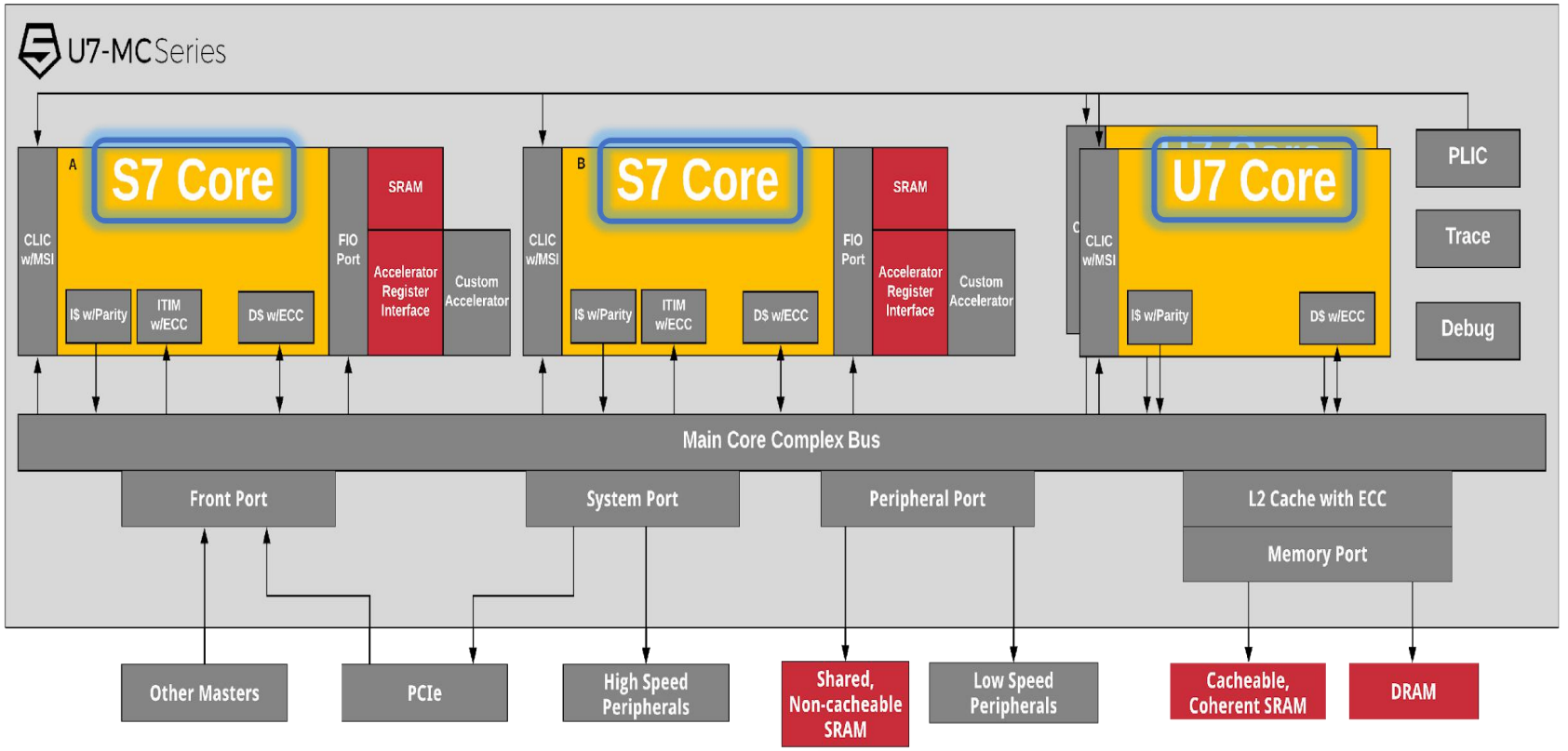
AR/VR/Sensor Fusion

App + Real-Time Processors - Coherent in-cluster combinations

App processors
Run high performance Linux and user apps

Simple caching hierarchy for ease of application optimization

Low Latency peripheral access

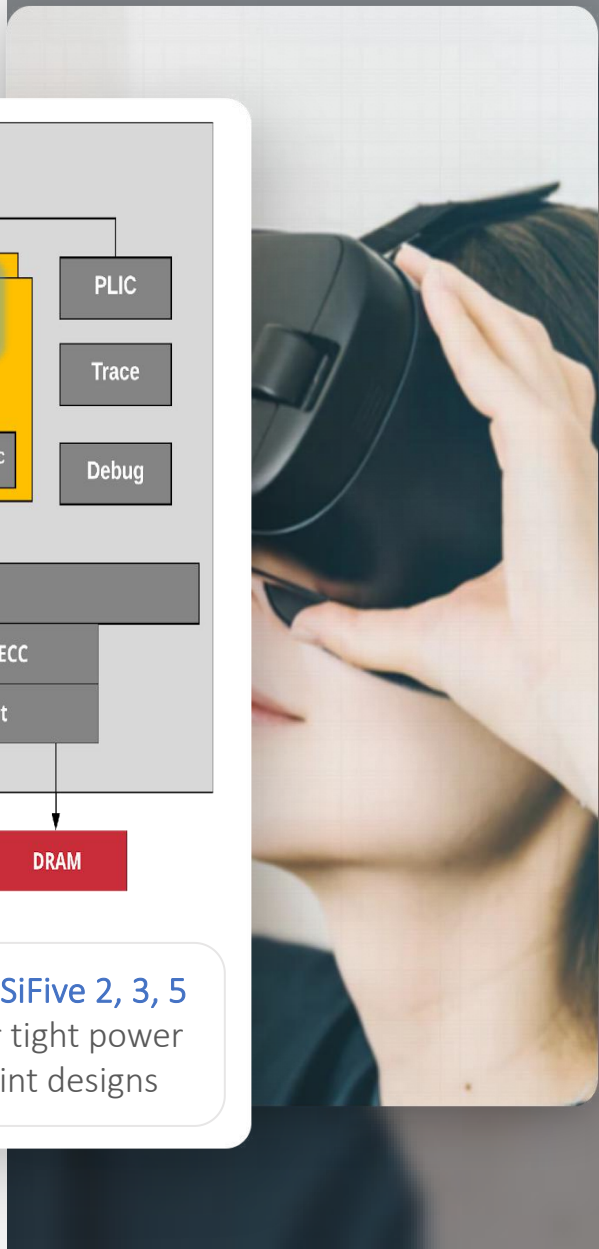


AR/VR/MR/CV Workloads
Accelerators, vector extensions, SCIE

Mixed precision arithmetic for accelerating machine learning compute

64-bit addressability and scalar compute for complex graphics

Use with SiFive 2, 3, 5 series for tight power constraint designs



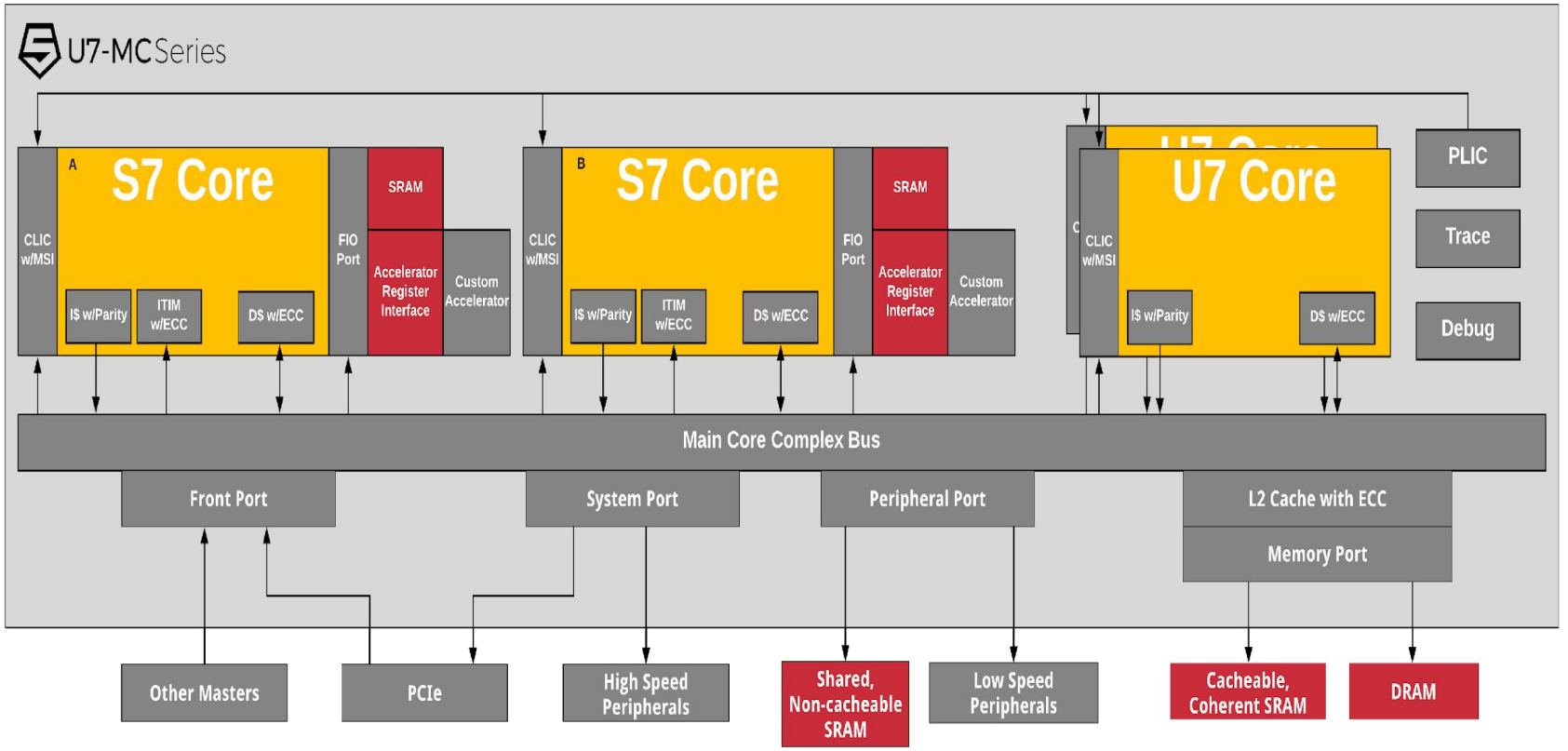
AR/VR/Sensor Fusion

App + Real-Time Processors - Coherent in-cluster combinations

App processors
Run high performance Linux and user apps

Simple caching hierarchy for ease of application optimization

Low Latency peripheral access

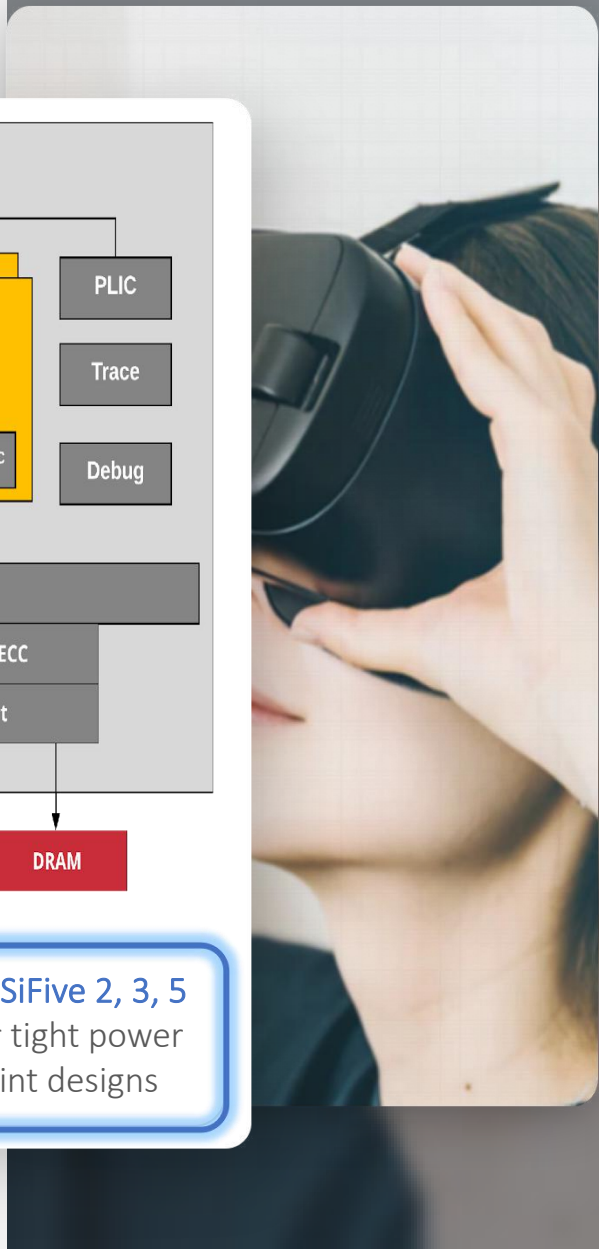


AR/VR/MR/CV Workloads
Accelerators, vector extensions, SCIE

Mixed precision arithmetic for accelerating machine learning compute

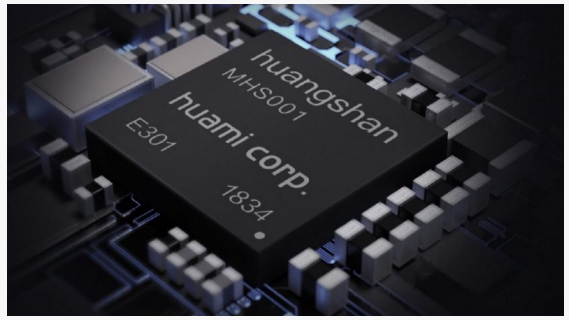
64-bit addressability and scalar compute for complex graphics

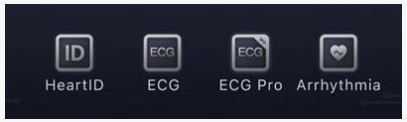
Use with SiFive 2, 3, 5 series for tight power constraint designs



Recently announced products

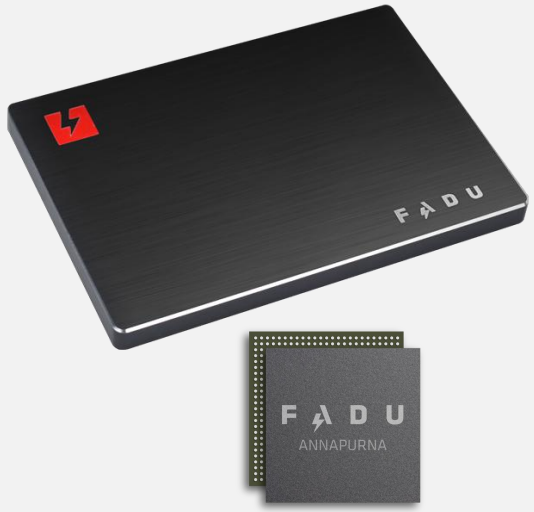
Wearable AI





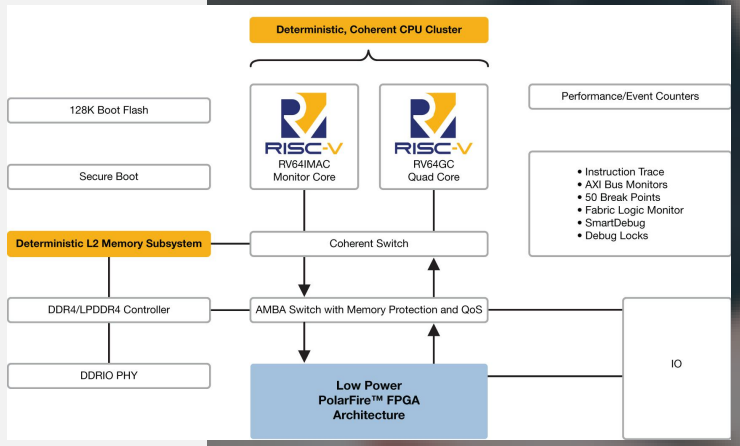
huami

Enterprise



FADU

Edge



Microsemi
a MICROCHIP company

Rapid adoption of SiFive Core IP from the Edge to the Core

SiFive – the Broadest Embedded Core IP Portfolio

	E Cores — 32-bit embedded cores: MCU, edge computing, AI, IoT	**S Cores** — 64-bit embedded cores: Storage, AR/VR, machine learning	**U Cores** — 64-bit application cores: Linux, datacenter, network baseband
7 Series — **Highest performance:** 8-stage, dual-issue superscalar pipeline	**E7 Series**	**S7 Series**	**U7 Series**
	E76-MC — Compare to Cortex-M7 Quad-core 32-bit embedded processor	**S76-MC** — No 64-bit Cortex equivalent Quad-core 64-bit embedded processor	**U74-MC** — Compare to Cortex-A55 MP4 Multicore: four U74 cores and one S76 core
	E76 — Compare to Cortex-M7 High performance 32-bit embedded core	**S76** — No 64-bit Cortex equivalent High-performance 64-bit embedded core	**U74** — Compare to Cortex-A55 High performance LInux-capable processor
3/5 Series — **Efficient performance:** 5–6-stage, single-issue pipeline	**E3 Series**	**S5 Series**	**U5 Series**
	E34 — Compare to Cortex-R5F E31 features + single-precision floating point	**S54** — No 64-bit Cortex equivalent S51 features + single-precision floating point	**U54-MC** — Compare to Cortex-A53 Multicore application processor with four U54 cores and one S76 core
	E31 — Compare to Cortex-R5 Balanced performance and efficiency	**S51** — No 64-bit Cortex equivalent Low-power 64-bit MCU core	**U54** — Compare to Cortex-A53 Linux-capable application processor
2 Series — **Power & area optimized:** 2–3-stage, single-issue pipeline	**E2 Series**	**S2 Series**	
	E24 — Compare to Cortex-M4F E21 + single-precision floating point	**S21** — No 64-bit Cortex equivalent Area-efficient 64-bit MCU core	
	E21 — Compare to Cortex-M4 E20 + User Mode, Atomics, Multiply, TIM		
	E20 — Compare to Cortex-M0+ Our smallest, most efficient core		

SiFive

Rich Portfolio of IP : Internal IPs + Partner IPs

300+
Tape outs
1500+
Unique IP
Integrated

SerDes

- CEI-11G, 25/28G, 56G, 112G
- JESD204B/C
- CPRI
- PCI Express 1/2/3/4/5
- XAUI, XFI, 10G-KR
- High Speed Memory
- xGMII
- SATA / SAS
- USB2.0/3.0/3.1
- Infiniband
- High Speed Backplane
- Rapid I/O
- HT
- DVI
- OBSAI
- Fibre Channel
- SPI4-2, SPI5
- SFI4-2

Analog / Wireless

- Nyquist ADC/DACs
- Sigma/delta ADC/DACs
- PLLs/Synthesizers
- Fractional PLL
- DLLs
- WLAN AFE
- Custom AFE
- Audio CODEC ADC

Analog / Wireless

- PVT sensing
- POR
- Voltage detection
- Voltage references
- Bluetooth AFE
- Video DAC/ADC
- DC-DC converters
- LDO voltage regulators

Interface & Soft-IP

- PCIe Controller
- USB Controller
- I^2C/I^2S
- UART, WDT, RTC
- AMBA Peripherals
- Primecells
- DesignWare
- PCI, PCI-X, PCIe
- Ethernet MAC
- HDMI, MHL, eDP/DP
- UWB
- High Speed Memory Controller
- MIPI, SMIA, MDDI
- UHS, SD Controllers

Processor/DSP

- SiFive RISC-V cores
- ARM Cores
- ARM Mail GPU
- Synopsys/ARC
- Imagination
- Cadence/Tensilica
- CEVA DSP
- Custom AI Accelerators

Standard Cell Libraries

- ARM/Artisan
- TSMC
- Synopsys/Virage
- Dolphin
- High Performance Kits

Memories

- SRAM (HS, HD, UHD, LP)
- Register Files
- ROM (Metal/VIA/Diff)
- Efuse
- ECC and Repair
- CAM/TCAM
- 1T-SRAM
- OTP/MTP
- eflash

Specialty IO's

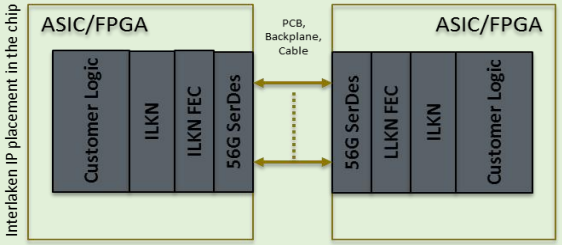
- LPDDR5/4
- DDR4/3
- GDDR6
- LVDS
- HSTL 1.8/1.5
- QDR
- SSTL-2/18/15
- PCI, PCI-X 1.0
- PCI-X 2.0
- USB 1.1
- GMII/RGMII
- PECL
- CML
- I^2C
- I3C
- Multi-voltage
- Oscillator IO
- MFIO (LVCMOS, SSTL, HSTL)

Differentiated IP Solutions

Interlaken IP Subsystem

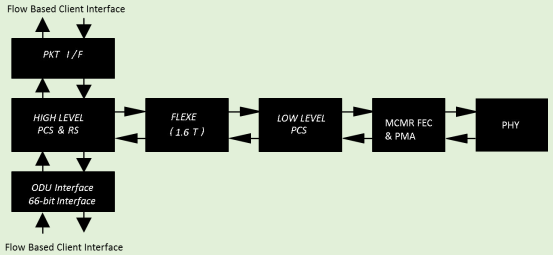
ILKN & ILKN FEC

- #1 Provider in market
- 75+ IP licenses
- Works with up to 48 parallel physical SerDes lanes 3.125 Gbps to 112 Gbps speeds
- Supports bandwidth of up to 1.2 Tbps



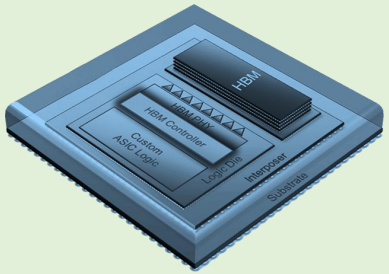
Ethernet IP Subsystem

- **400/200/100/50/25GbE** MAC+ PCS+ FEC IP
- Integrated with various SerDes in 16nm and 7nm
- Flex IP for Optical Transport market



High Bandwidth Memory (HBM) IP Subsystem

- IP subsystem solution (**Controller + PHY+ I/O**)
- HBM2 IP availability since Q4 2015
- Silicon Proven IP
- IP available in **22FDx, 16nm, 14nm and 7nm**
- Received Customers' Choice Award for best paper at TSMC NA OIP 2017



SiFive Core IP: Embedding Intelligence Everywhere

Efficient Performance

Scalability

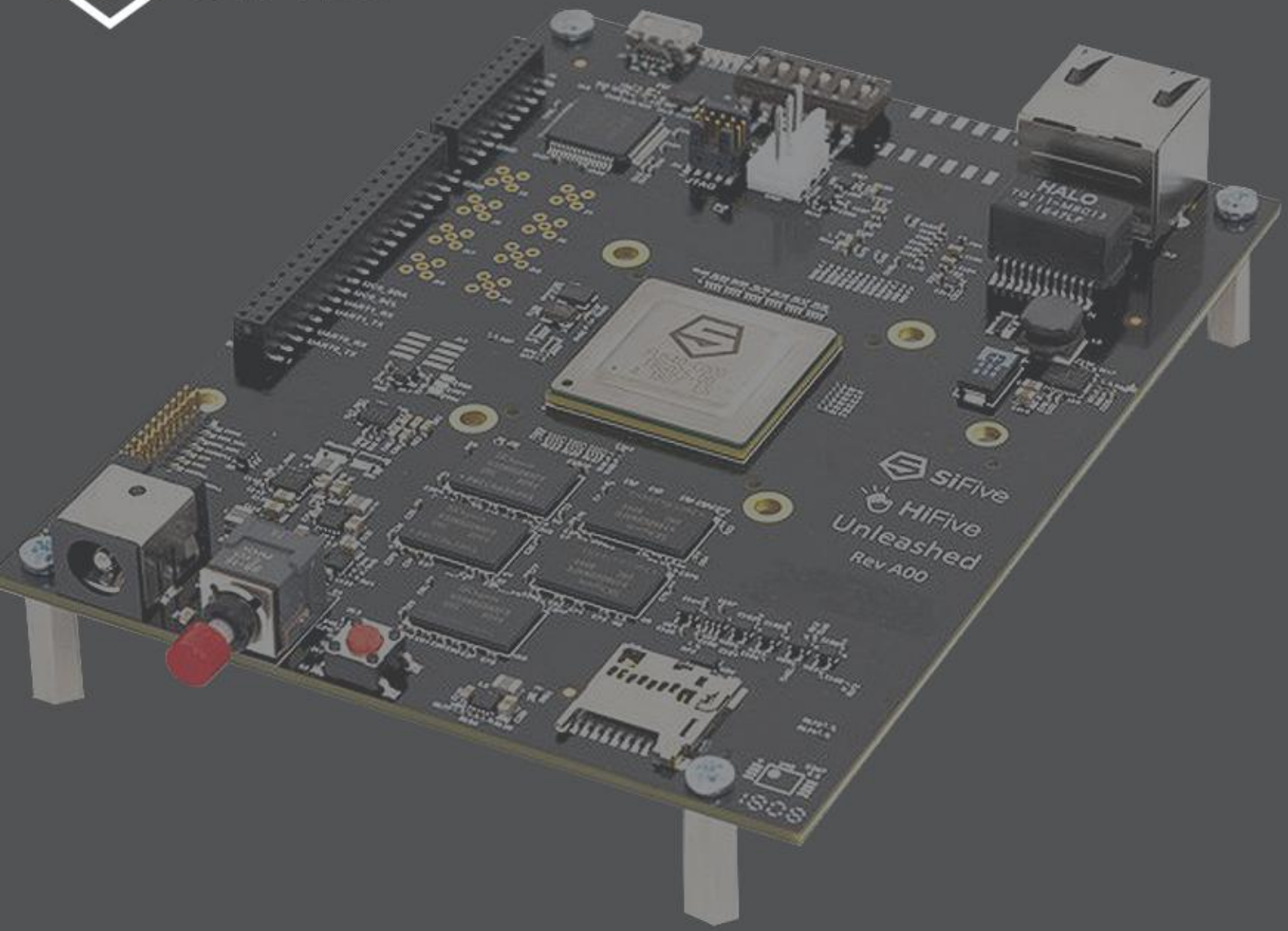
Differentiating Feature Set

→

Embedding intelligence for a world of a Trillion Connected Devices

SiFive

SiFive



Silicon verified. Market proven.

The most advanced configurable core IP and silicon solutions from the inventors of RISC-V.

Microcontrollers ▪ Embedded ▪ Linux ▪ Multicore

▪ Networking ▪ Storage ▪ Computing ▪ AI
▪ Industrial ▪ IoT ▪ Consumer ▪ Automotive

www.sifive.com