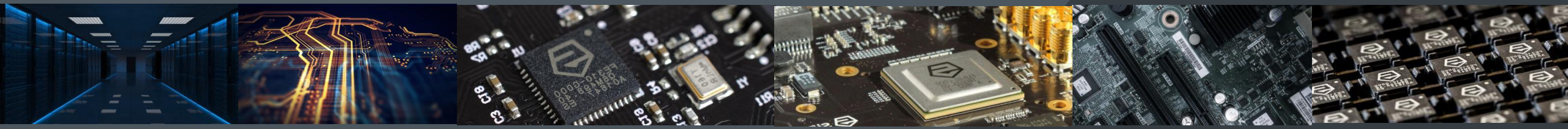
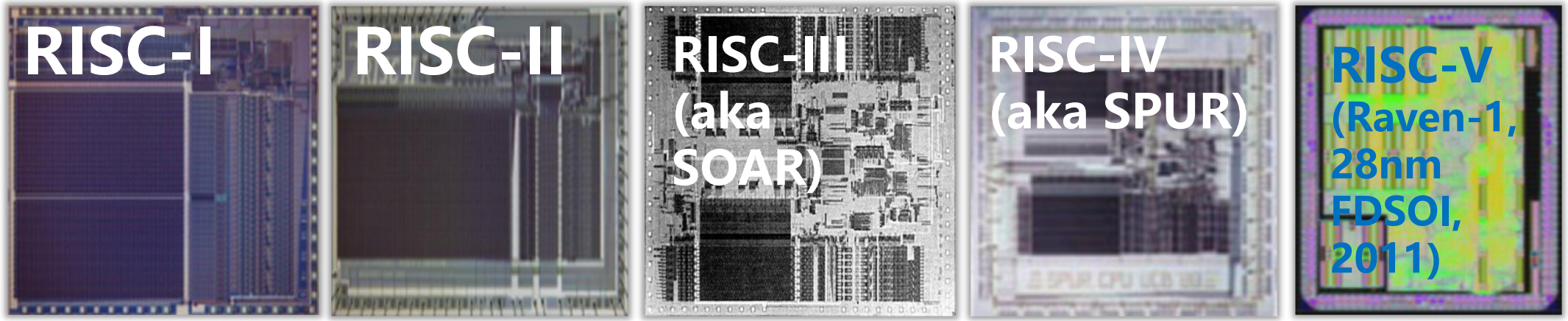
RISC-V 的历史和机遇



周 杰　赛昉科技销售总监
jie.zhou@sifive.com
2019.10

什么是RISC-V?

A license-free and royalty-free
High-quality, *Modular*
Suitable for all types of computing system,
ISA specification,
Originally from UC Berkeley



RISC-V®

SiFive

David Patterson

Google杰出工程师 & SiFive 技术顾问

Andrew Waterman

SiFive 联合创始人 & 首席工程师

Yunsup Lee

SiFive 联合创始人 & CTO

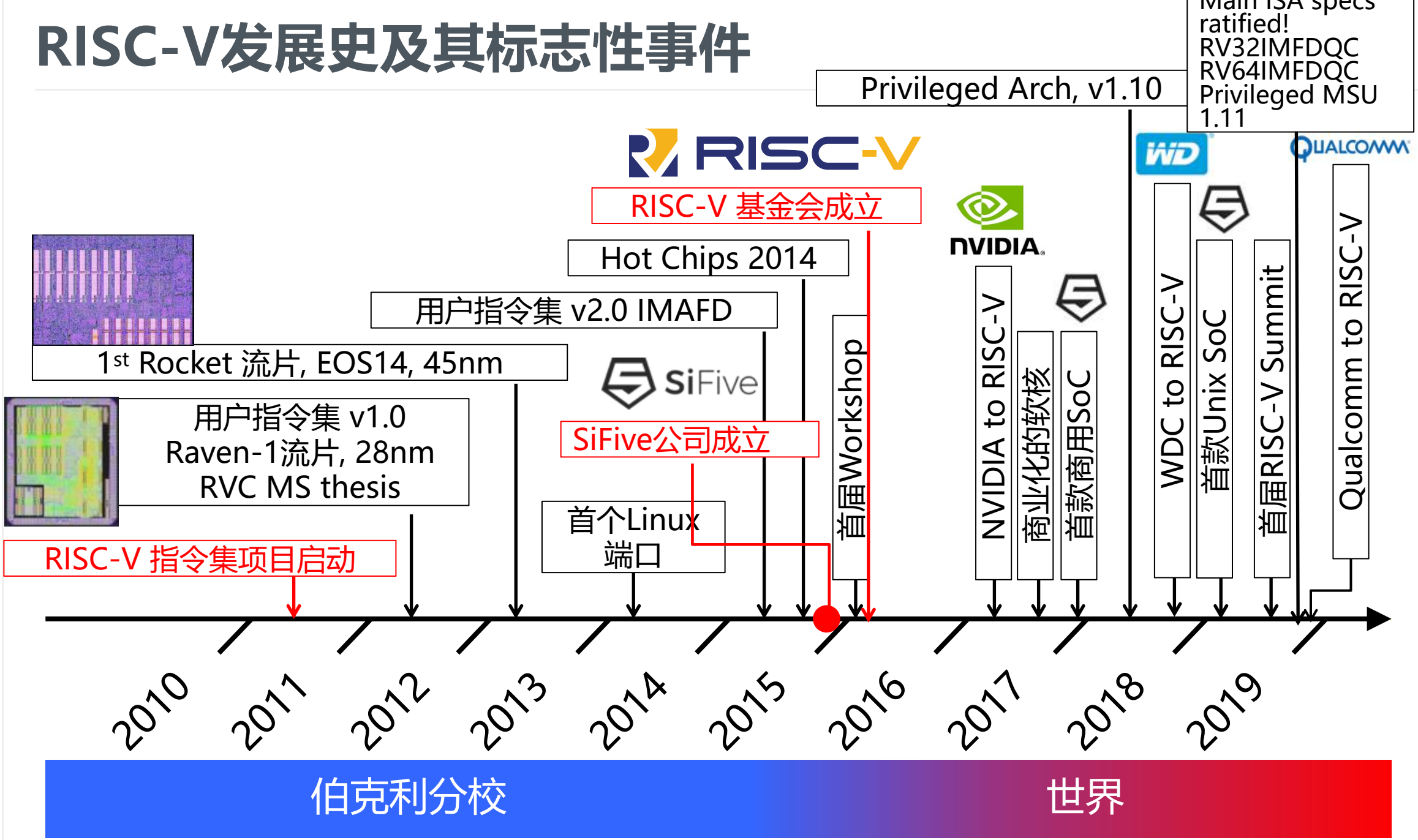
Krste Asanovic

SiFive 联合创始人 & 首席架构师

我们发明了RISC-V

我们成立了SiFive

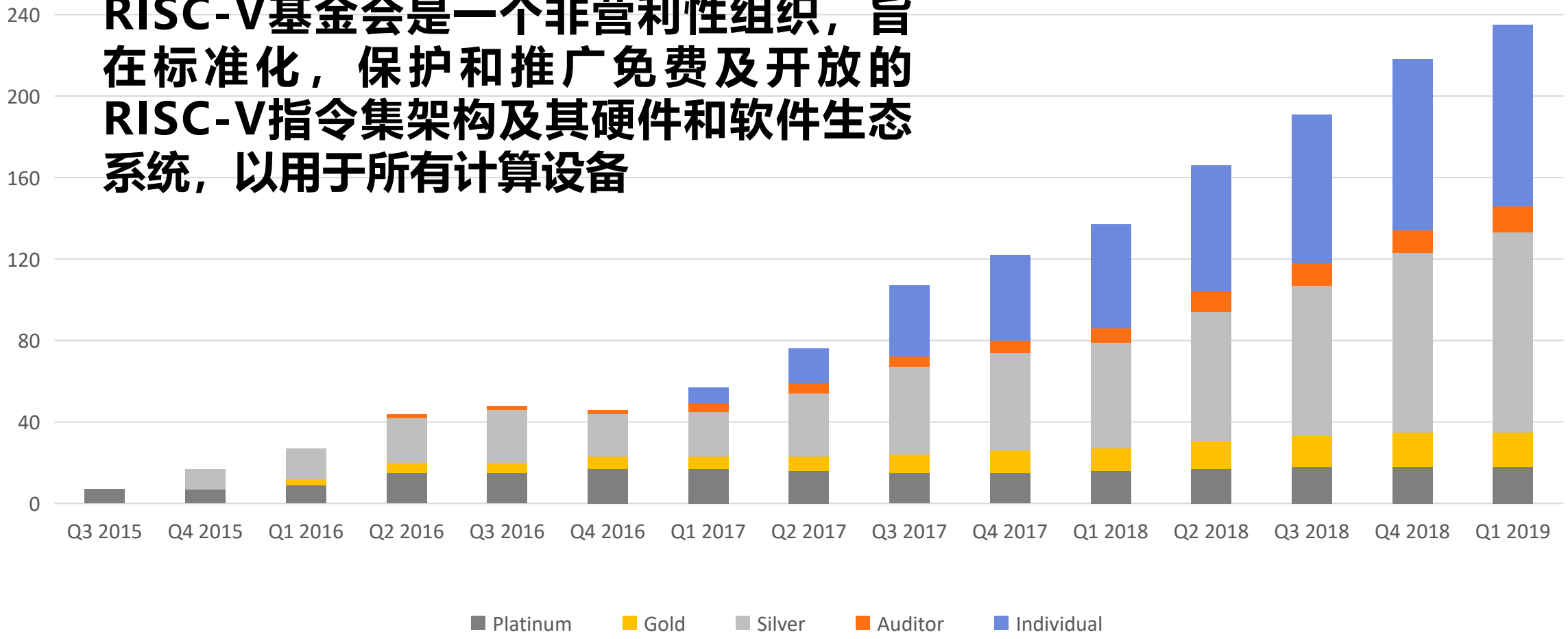
RISC-V发展史及其标志性事件

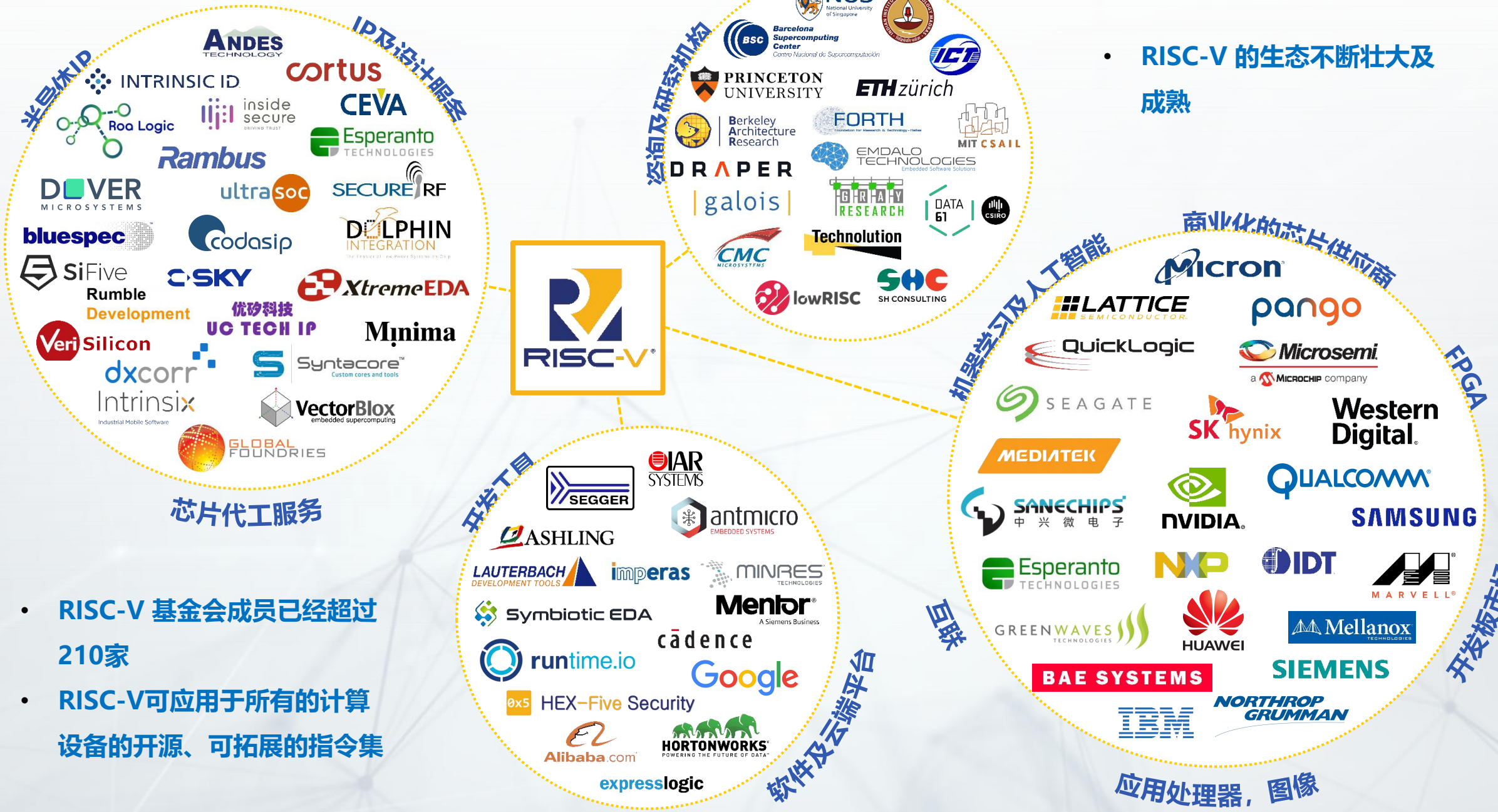


RISC-V 基金会成员的快速增长

从2015年9月至2019年2月

RISC-V基金会是一个非营利性组织，旨在标准化，保护和推广免费及开放的RISC-V指令集架构及其硬件和软件生态系统，以用于所有计算设备





- RISC-V 的生态不断壮大及成熟

- RISC-V 基金会成员已经超过210家
- RISC-V可应用于所有的计算设备的开源、可拓展的指令集

RISC-V基金会工作群组

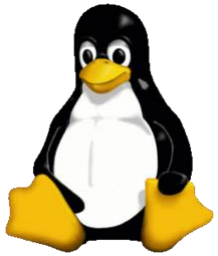
Compliance

Technical Deliverables

Opcode Space Mgmt Standing Committee
Software Standing Committee
Security Committee
Base ISA Ratification Task Group
Privileged ISA Spec Task Group
Formal Specification Task Group
Trusted Execution Env Spec Task Group
B Extension (Bit Manipulation) Task Group
J Extension (Dynam. Translated Lang) Task Group
P Extension (Packed-SIMD Inst) Task Group

V Extension (Vector Ops) Task Group
Cryptographic Extension Task Group
Debug Specification Task Group
Fast Interrupts Spec Task Group
Memory Model Spec Task Group
Processor Trace Spec Task Group
Sv128 Specification Task Group
Compliance Task Group
UNIX-Class Platform Spec Task Group
Safety Task Group (Proposed)

RISC-V开源软件生态进展



Software	Status	Recommended source release	Notes
GCC	Upstreamed as of 7.1	Upstream or SiFive: https://github.com/sifive/freedom-tools	SiFive maintains binary and source distributions which may contain patches which have not be upstream yet
LLVM	Upstreamed in experimental mode as of 8.0.	https://github.com/llvm-mirror/llvm	Non-experimental support planned for 9.0 release
GDB	Upstreamed as of 8.2	https://github.com/riscv/riscv-gnu-toolchain	
binutils	Upstreamed as of 2.28	Upstream	
newlib	Upstreamed as of 2.5.0	Upstream	
glibc	Upstreamed as of 2.27	Upstream	
Linux Kernel	Upstreamed as of 4.15	Upstream or SiFive: https://github.com/sifive/riscv-linux	
qemu	Upstreamed as of 2.12	Upstream	
OpenOCD	Upstreamed	https://github.com/riscv/riscv-openocd	

RISC-V商业生态进展 （部分列举）

SiFive Freedom SDK
- GCC+ BinUtils

SiFive Freedom Studio
- Freedom SDK, Eclipse CDT, GNU MCU Eclipse, pre-built GCC, and OpenOCD
- Built on Open Source technology

UltraSoC
- IP and tooling supporting SiFive instruction trace

Lauterbach
- Lauterbach TRACE32 for silicon bring up and debug

Imperas
- Simulation models and tools for early S/W development

IAR
- IAR Embedded Workbench with SiFive support in development

SEGGER
- SEGGER JLINK for Debug and Production Flash Programming
- Embedded Studio for RISC-V – IDE, toolchain, debugger

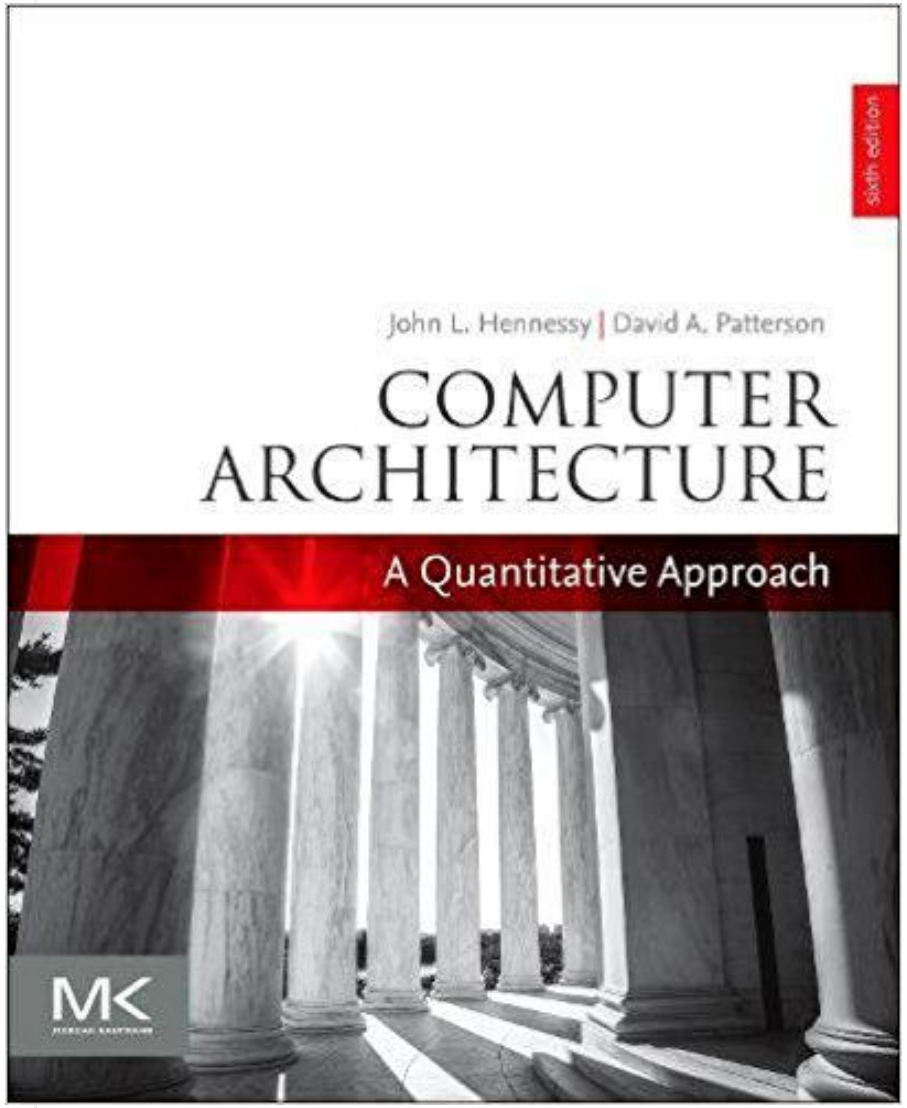
Embedded Operating Systems
- RT-Thread
- Express Logic – Thread X
- FreeRTOS
- Zephyr OS
- Micrium - µCOS
- RIOT
- NuttX

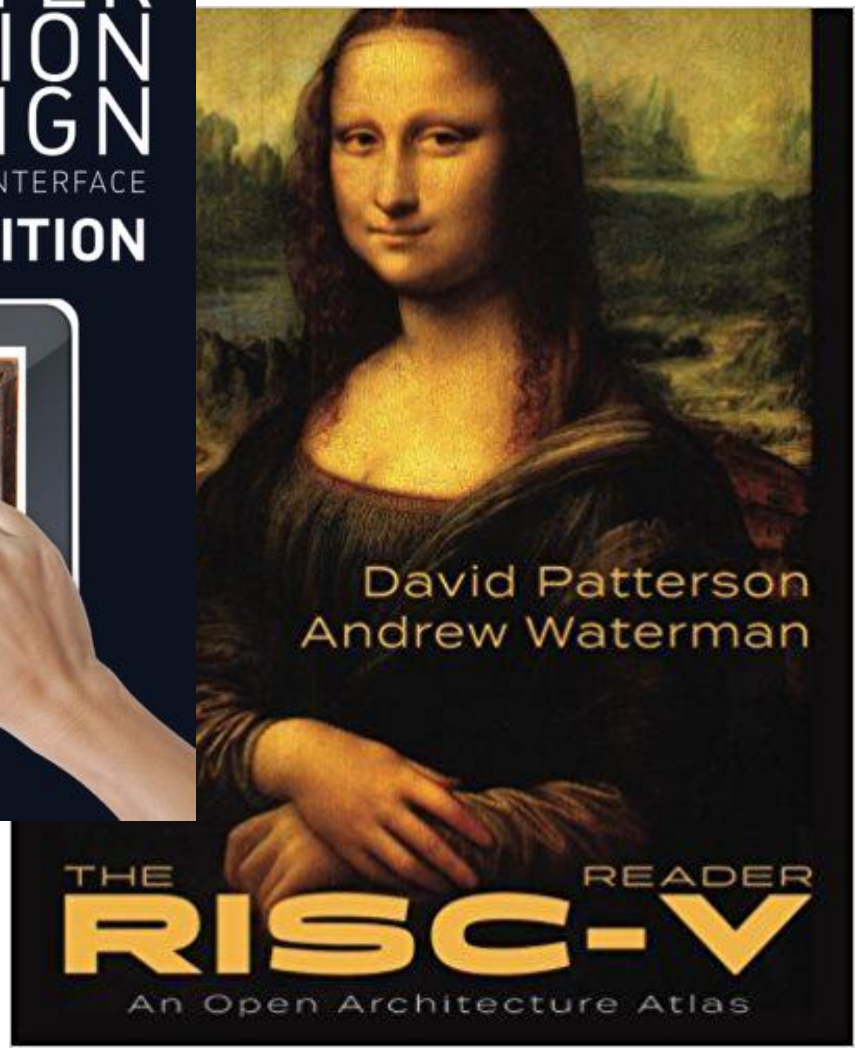
Rich Operating Systems
- Debian Linux
- Fedora Linux
- SylixOS
- VxWorks

RISC-V业界进展

- **拥抱RISC-V**
  - Andes, Codasip, Cortus ,Pintouge, Nuclei, Syntacore等宣布基于RISC-V的IP核产品线
- **开发板和生态系统**
  - SiFive推出开源CPU IP Rocket以及开源平台Rocket -chip ， 并推出 Freedom Everywhere (IoT), Freedom Unleashed (高性能)开发板, 作为软件和应用开发平台
  - Microsemi / NXP 推出开发板
  - Western Digital推出开源RISC-V核 SweRV
  - Nuclei推出1分钱计划 / Andes 推出FreeStart计划 / 平头哥宣布玄铁910 并推出CPU开放普惠计划
- **政府和研究机构**
  - 伯克利--清华在深圳成立RIOS实验室
  - 上海经信委针对基于RISC-V的芯片项目成立专项资金
  - 印度政府投资 $90M/$40M 在RISC-V CPU项目，已经推出6款不同等级的RISC-V处理器
- **芯片产品**
  - 紫光展锐宣布推出两款采用RISC-V技术的春藤系列蓝牙耳机芯片
  - 汇顶科技宣布推出采用RISC-V技术的智能门锁方案

RISC-V学界进展

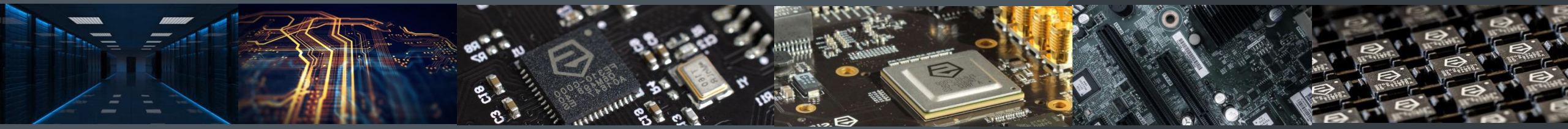




RISC-V spreading quickly throughout curricula of top schools

SiFive

SiFive推动RISC-V技术创新与发展



SiFive是RISC-V标准制定的主要贡献者

Bit Manipulation

Compliance

Debug

Memory Model

Privileged Spec

Vector

Security

Base ISA / Opcode

SiFive 推动 RISC-V 开源生态的发展

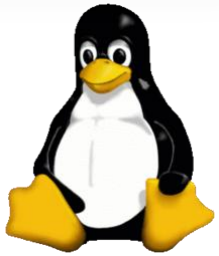
SiFive是最重要的RISC-V开源软件贡献者

- GCC 主要的贡献者 - Palmer, Kito
- GDB主要的贡献者 - Palmer
- Linux Kernel 主要的贡献者 - Palmer, Albert, Greentime
- QEMU 主要的贡献者 – Michael Clark
- Binutils 主要的贡献者 - Palmer, Jim, Andrew
- OpenOCD主要的贡献者 – Tim, Megan, Palmer

https://riscv.org/software-status/

由SiFive领导的其他RISC-V开源项目

- Linux, FreeRTOS, Zephyr, GNU MCU Eclipse, Spike….



SiFive Freedom SDK

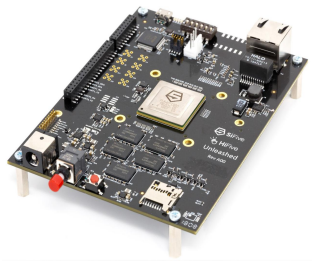
- GCC+ BinUtils

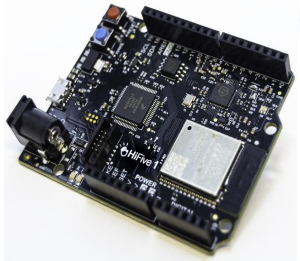
SiFive Freedom Studio

- Freedom SDK, Eclipse CDT, GNU MCU Eclipse, pre-built GCC, and OpenOCD
- Built on Open Source technology

SiFive Dev board

- **HiFive1** - Embedded RISC-V Dev Board compliant to Arduino
- **SiFive HiFive Unleashed** - World’s First Multi-Core RISC-V Linux Dev Board

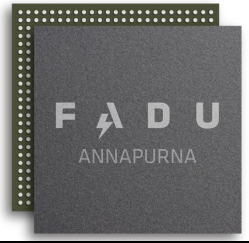




SiFive 领导 RISC-V产业界的发展

- 西数宣布和SiFive合作，将把高达每年20亿颗的芯片转向基于RISC-V
- Microsemi推出基于SiFive 核的FPGA产品
- 嘉楠推出基于SiFive 开源核的AI Kendryte 芯片
- 比特大陆推出基于SiFive 开源核的AI芯片
- Fadu 宣布基于SiFive 核的SSD 控制器芯片
- 英伟达宣布推出基于SiFive 开源核的产品
- SiFive, Google, WD等成立CHIPS联盟
- 华米–推出基于SiFive 核的边缘AI计算芯片黄山一号量产，其智能手表已开始供货
- Redhat基于SiFive unleashed board将Fedora移植到RISC-V

- 西数、英特尔、高通投资SiFive助力RISC-V在产业界推广
- 全球前10大半导体公司6家采用SiFive商用RISC-V IP
- 100多个基于SiFive 商业核的芯片项目正在开发中



SiFive在全球范围内推动RISC-V生态发展

Year 2018	Year 2019
15 Cities	75 Cities
22 City Tours	
55 Talks	350 Talks
8,000 Attendees	
2,500,000 Video Views	6,000,000 Video Views

SiFive

USA
Feb 21 – Austin
Fab 26 – Mountain View
Feb 28 – Boston

EUROPE
May 10 – Cambridge
May 15 – Grenoble
May 17 – Stockholm
May 20 – Moscow
May 23 – Munich
May 29 – Amsterdam

APAC & AUSTRALIA
Jun 11 – Tokyo
Jun 13 – Pangyo
Jun 14 – Daejeon
Jun 17 – Taipei
Jun 19 – Singapore
Jun 21 – Sydney

CHINA (Technical Workshops)
Mar 29 – Shanghai
Jun – Shenzhen
Aug – Beijing

PAKISTAN
Jul 29 – Islamabad
Jul 30 – Karachi
Jul 31 – Lahore

INDIA & BANGALESH
Aug 1 – Noida
Aug 2 – Pune
Aug 3 – Mumbai
Aug 5 – Bangalore
Aug 7 – Kolkata
Aug 8 – Dhaka
Aug 10 – Chennai
Aug 13 – Hyderabad

USA
Aug 21 – NYC
Aug 23 – San Diego
Aug 27 – Portland
Aug 28 – Seattle
Aug 29 – Palo Alto

MEA
Sep 2-6 – Tel Aviv
Sep 2-6 – Cairo
Sep 2-6 – Dubai
Sep 2-6 – Istanbul

CHINA
Oct 21-31 – Suzhou
Oct 21-31 – Xi`an
Oct 21-31 – Chengdu
Oct 21-31 – Wuhan
Oct 21-31 – Beijing
Oct 21-31 – Shenzhen

MEXICO & SOUTH AMERICA
Nov 18-29 – Mexico City
Nov 18-29 – Medellin
Nov 18-29 – Sao Paulo
Nov 18-29 – Florianopolis
Nov 18-29 – Santiago
Nov 18-29 – Buenos Aires

SiFive推动RISC-V CPU IP产品的创新

U Cores

64-bit Application Processors

S Cores

64-bit Embedded Processors

E Cores

32-bit Embedded Processors

Embedding Intelligence from the Edge to the Cloud

SiFive推动IP定制、验证、交付方式的创新 -- 云平台

Product Specific, Unique Requirements

Features | Power | Performance | Area

Web Interface

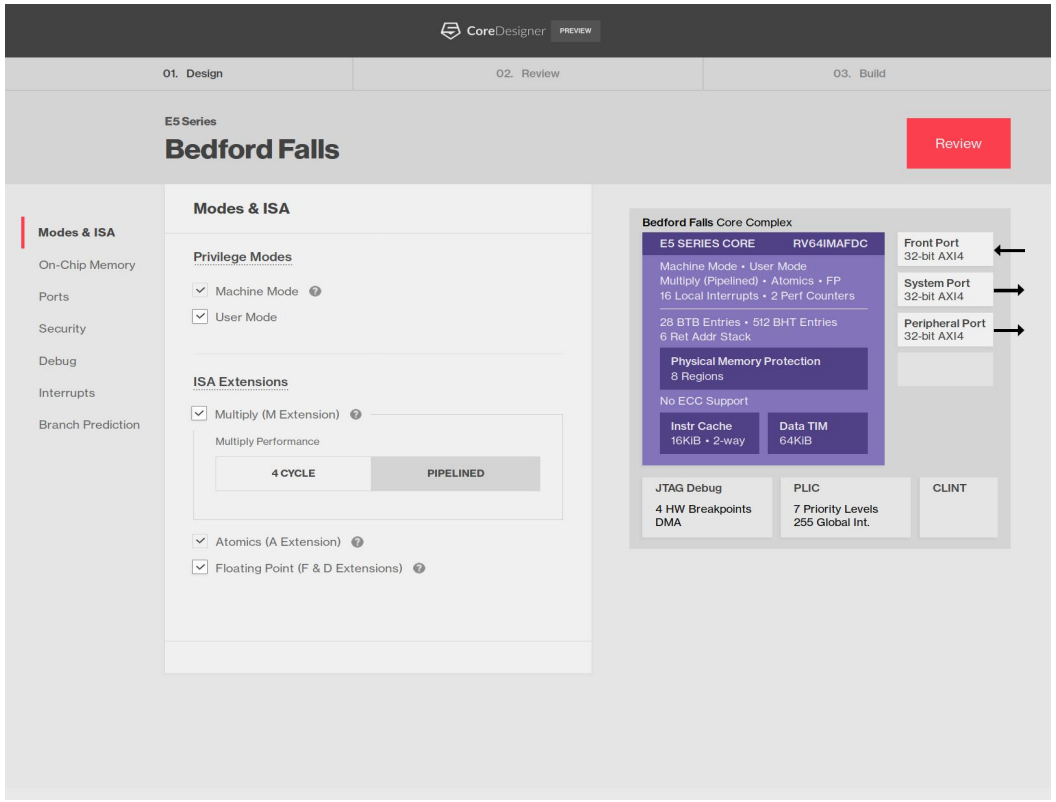
SiFive Core Designer

Verilog RTL

Verified, Customized RISC-V IP

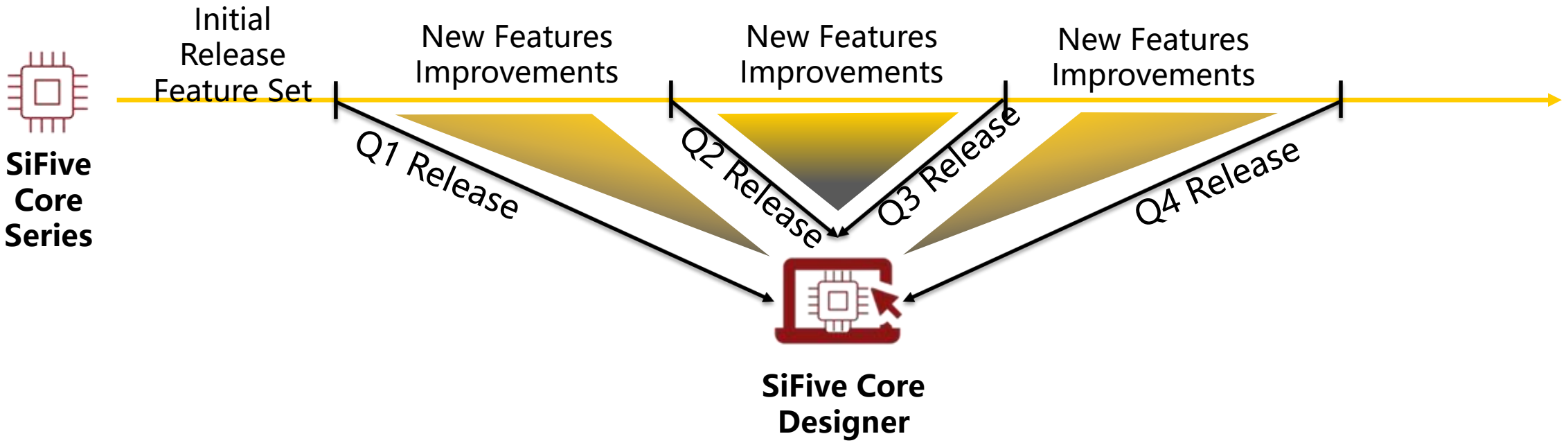
uControllers | Embedded | Linux | Multicore

Cloud-based
Customize your own RISC-V core
Unique for your application
Not shared with your competitors



SiFive推动IP更新方式的创新 – 季度上新

Regular, Predictable, Releases via SiFive Core Designer Like an APP



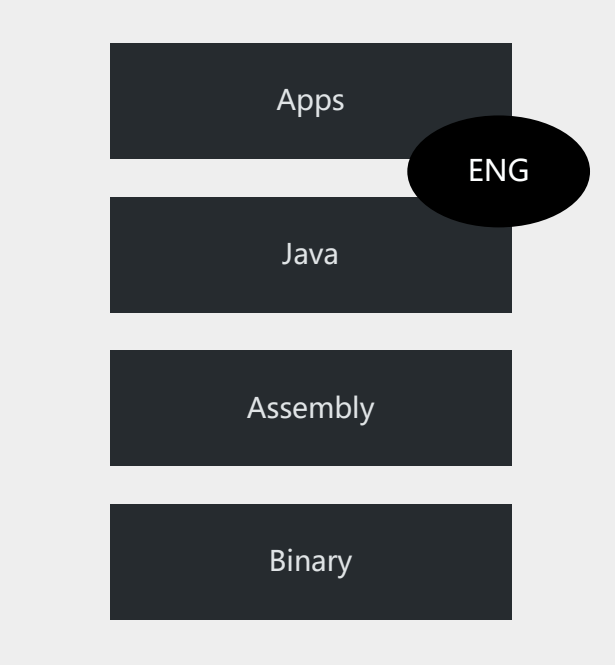
SiFive Core IP is configured via SiFive Core Designer’ s easy to use Web Interface

Subscriptions to Core Series grant access to new features over time

Core Series are verified to production quality for the defined feature set in a given release

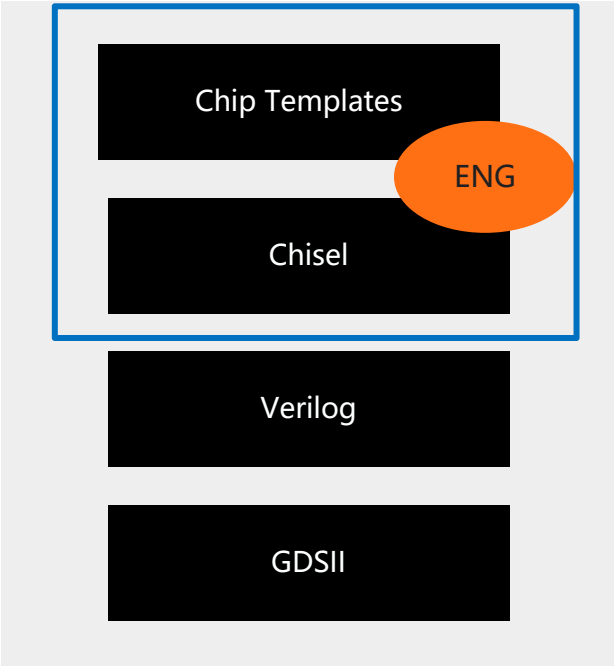
SiFive推动芯片设计创新 – 硬件堆栈

软件设计行业



芯片设计行业

芯片设计软件化革命



- **开发人员的关注领域的抽象程度大幅上升**
- **迭代周期大幅缩短**

芯片设计软件化	+	RISC-V技术	=	无限可能的IP核
芯片设计软件化	+	特定应用领域芯片 设计模板化	=	无限可能的芯片

We are More Than a RISC-V IP Provider

SiFive China

Contact Us

sales@sifive-china.com

marketing@sifive-china.com

recruitment@sifive-china.com

赛昉科技

- 最佳的RISC-V技术提供商和本土CPU IP的供应商
- RISC-V在中国生态发展的推动者
- 芯片设计创新方法与垂直应用平台整合的领导者
- 面向定制化处理器及芯片的基于云端SaaS 服务的先驱

周 杰 Jay

赛昉科技销售总监

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