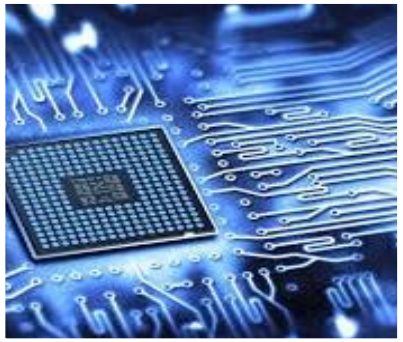
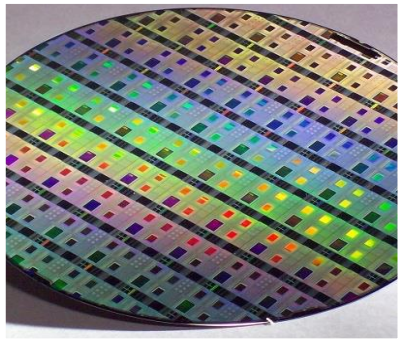
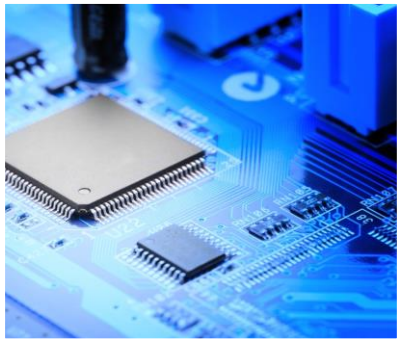
SiFive Tech Symposium 2019

SOC IP Solutions for Vertical Markets

Semiconductor IP World – Driving Trillion $ Market

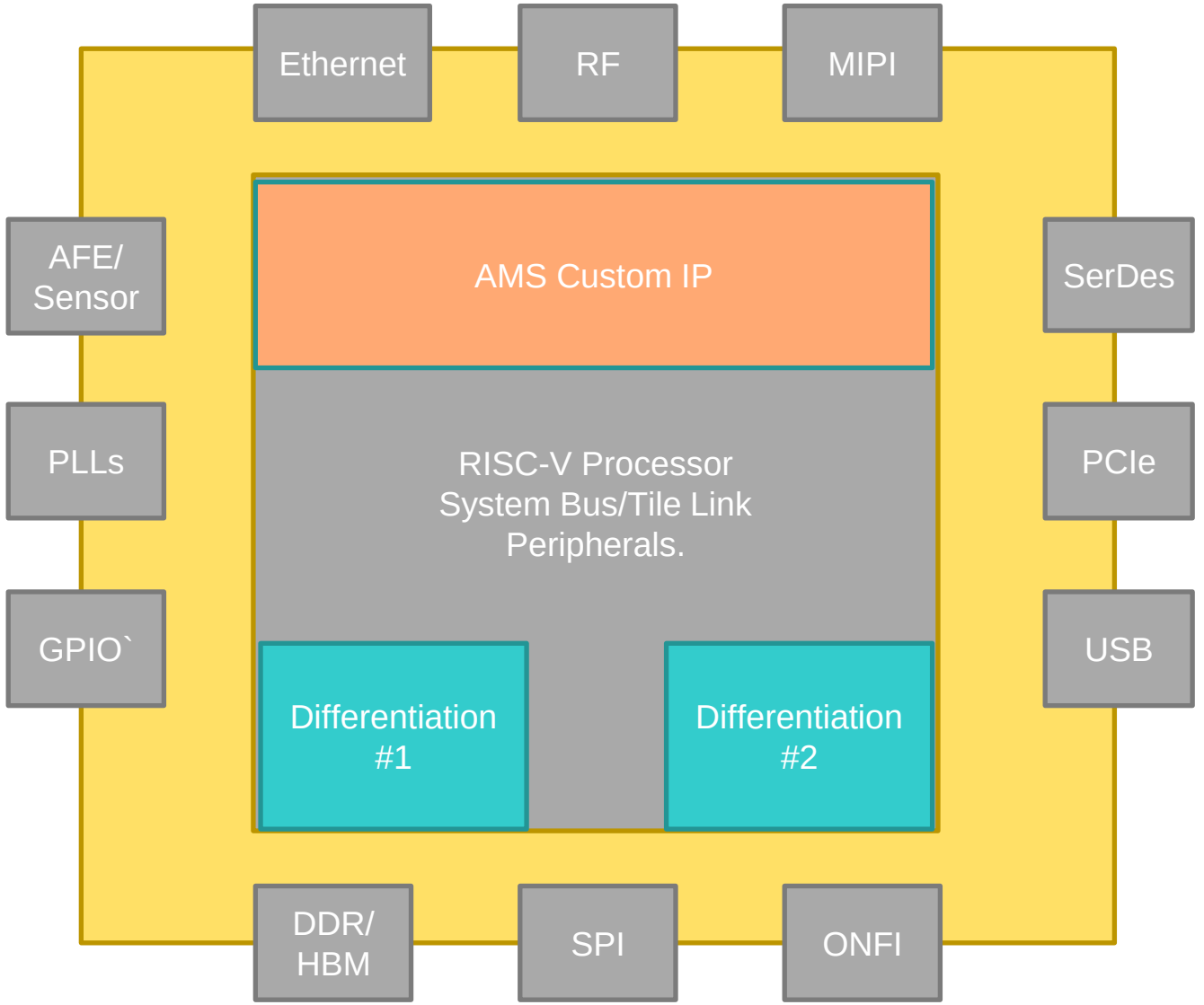
“IP” is Foundation to any Chip used in Electronics Systems

IP	Foundry	Semiconductors	Systems
			
$5B	$45B	$450B	$2T

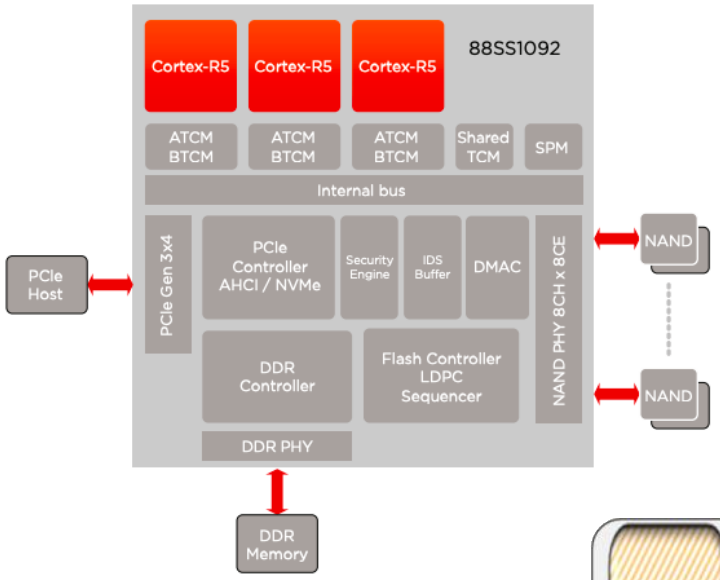
2021 estimates

SOC/ASIC Design Turning into IP Integration

- # of IP blocks per chip are growing
- Differentiation/Secret sauce/Custom IPs are typically application dependent
- Most start-ups don't have time to invent the wheel for IPs available from market
- For any semiconductor solutions company, IP is key to success



One Chip/Same IP Fits all applies? - NO

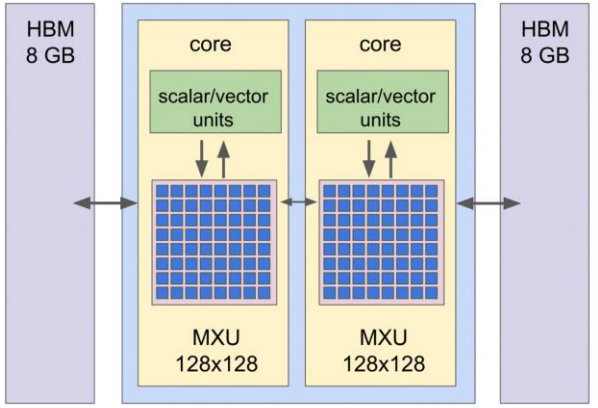


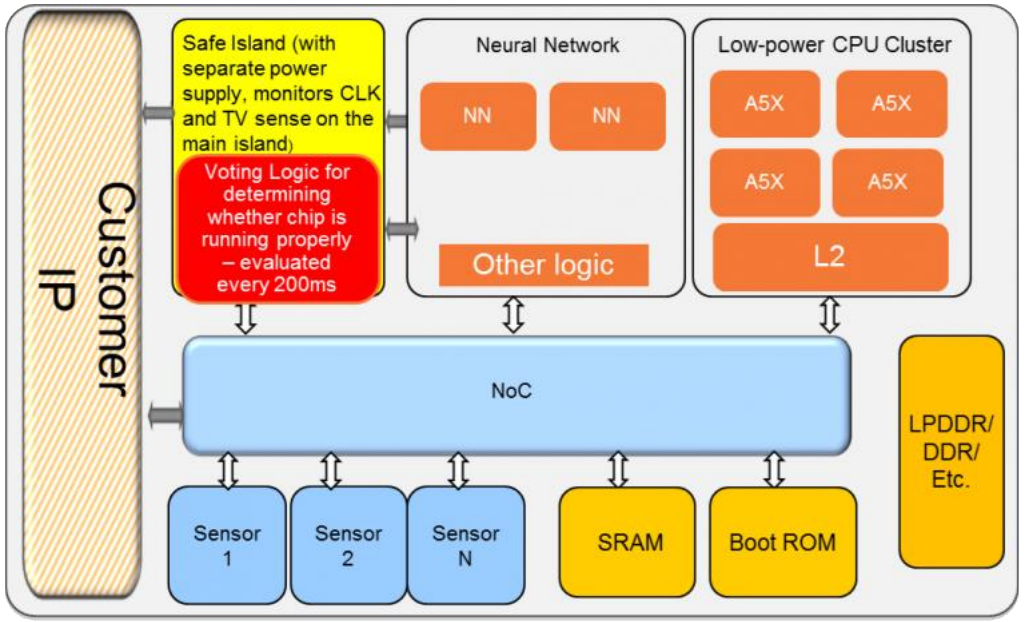
SSD Controller

AI/ML

TPUv2 Chip

- 16 GB of HBM
- 600 GB/s mem BW
- Scalar/vector units: 32b float
- MXU: 32b float accumulation but reduced precision for multipliers
- 45 TFLOPS



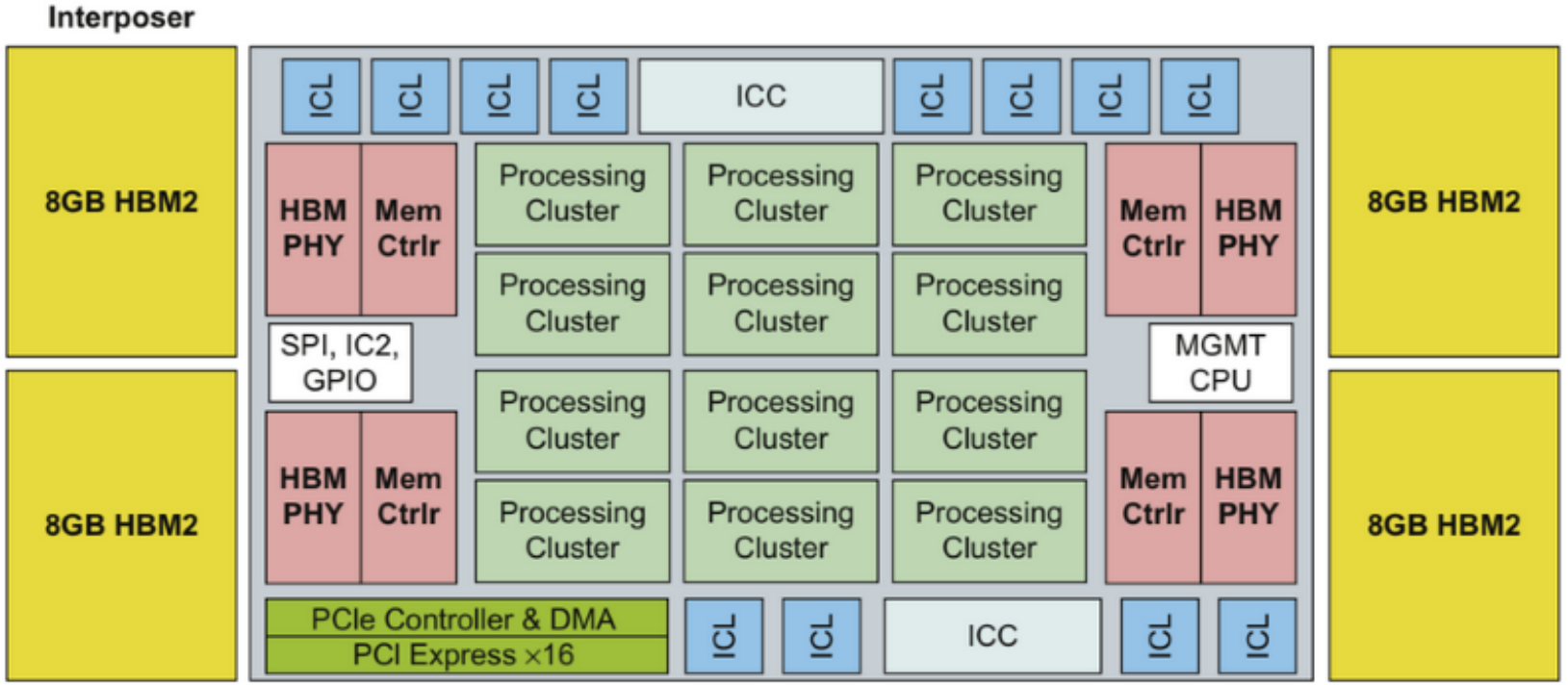


ADAS

Case Study #1: AI Accelerators

- GPUs, FPGAs, ASICs
- Lot of startups across the globe
- Semiconductor Growth driven by these devices

Key Q for many companies: We know Processing cluster/Neural Engine, Algorithms, how do I put the rest of chip? Technology node, power, Peripherals, Interfaces??



Source: Intel Nervana

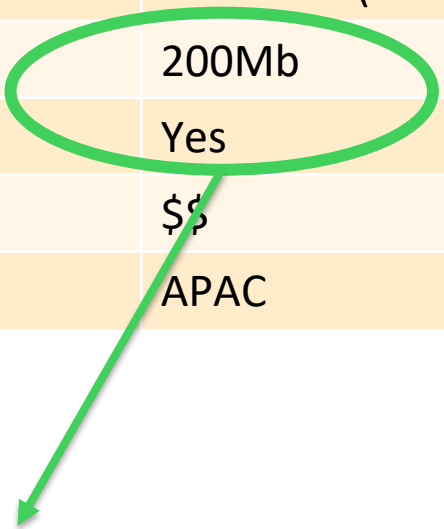
Example: Competing Memory Interface Technologies

	LPDDR4x	GDDR6	HBM2E
Interface Speed (Gbps)	4.2	14	3.2
Typ BW (Gbps)	273	448	3200
Power Eff (pJ/b)	2-3x	8x	1x
Area/Bit	7x	20x	1x
Cost	$	$$	$$$
Applications	Mobile, Consumer, Auto	GPU, AI	AI, HPC, Networking
Complexity	Low	Med	High

There is no Single memory technology for all chips!

Example: Optimized IP Solutions for Same application

	AI Customer #1	AI Customer #2
Foundry	14nm	16nm
Neural Engine	Internal	Internal
CPU	No	SiFive RISC-V
Memory Interface	LPDDR4 (Partner IP)	SiFive HBM2
PCIe	Gen4 x4 (Partner IP)	Gen4 x16 (Partner IP)
SRAMs	50Mb	200Mb
Custom SRAMs	No	Yes
Cost	$	$$
Market	US Customer	APAC

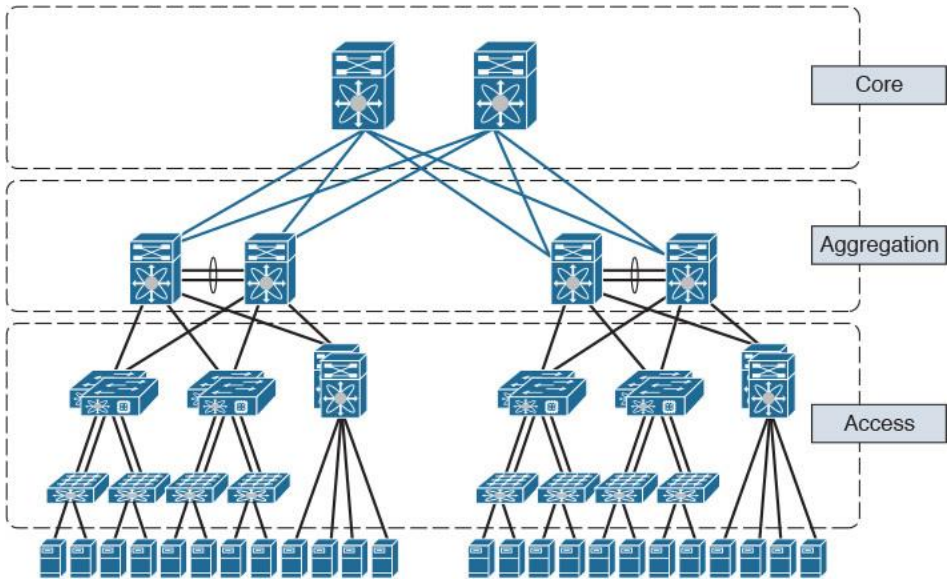


Custom 2Port SRAMs save 30% area and power on ASIC

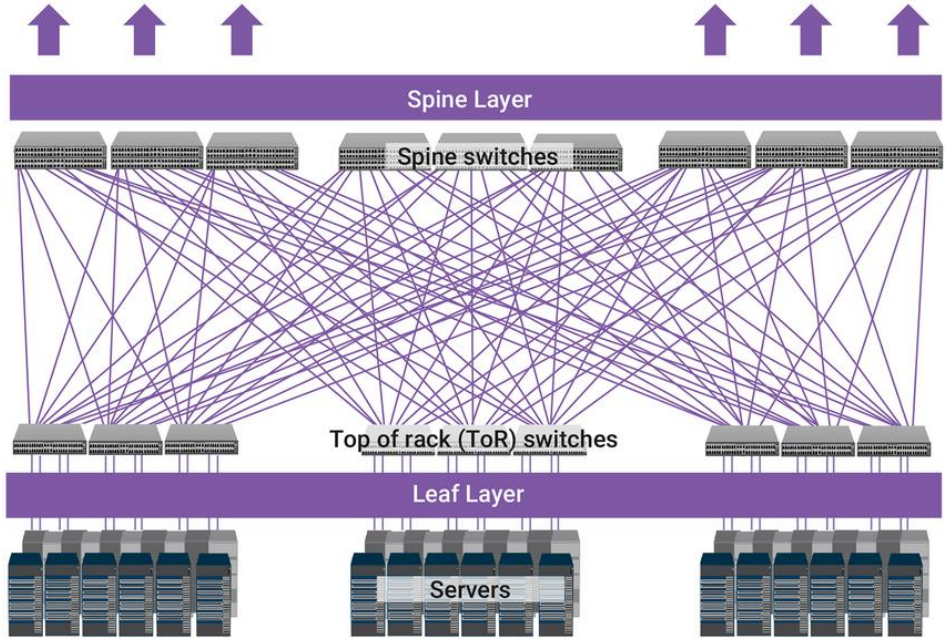
Case Study #2: Data Center Architecture

- Architectures are changing to support needs of High BW, Low Latency
- Drives the requirements on each ASIC for integration beyond Moore's Law!
- Power management is key aspect of any enterprise design

3-Tier Structure (NS Traffic)



2-Tier Structure (EW Traffic)



Examples: SerDes Technologies

	Ethernet – LR	Ethernet – MR, VSR	Die2Die - XSR
Interface Speed (Gbps)	10/25/56/112	10/25/56/112	80-112
Channels	35dB+	10-20dB	6-8dB
Power Eff (pJ/b)	5-7	3-5	1
Area	High	Med-High	Low
Applications	Backplane	C2C/C2M, Front panel	Chiplets, Optical integration
Complexity	High	Med	Low

Selecting right SerDes interface can help optimize Power & Area

Rich Portfolio of IP : Internal IPs + Partner IPs

300+
Tape outs
1500+
Unique IP
Integrated

SerDes

- CEI-11G, 25/28G, 56G, 112G
- JESD204B/C
- CPRI
- PCI Express 1/2/3/4/5
- XAUI, XFI, 10G-KR
- High Speed Memory
- xGMII
- SATA / SAS
- USB2.0/3.0/3.1
- Infiniband
- High Speed Backplane
- Rapid I/O
- HT
- DVI
- OBSAI
- Fibre Channel
- SPI4-2, SPI5
- SFI4-2

Analog / Wireless

- Nyquist ADC/DACs
- Sigma/delta ADC/DACs
- PLLs/Synthesizers
- Fractional PLL
- DLLs
- WLAN AFE
- Custom AFE
- Audio CODEC ADC

Analog / Wireless

- PVT sensing
- POR
- Voltage detection
- Voltage references
- Bluetooth AFE
- Video DAC/ADC
- DC-DC converters
- LDO voltage regulators

Interface & Soft-IP

- PCIe Controller
- USB Controller
- I^2C/I^2S
- UART, WDT, RTC
- AMBA Peripherals
- Primecells
- DesignWare
- PCI, PCI-X, PCIe
- Ethernet MAC
- HDMI, MHL, eDP/DP
- UWB
- High Speed Memory Controller
- MIPI, SMIA, MDDI
- UHS, SD Controllers

Processor/DSP

- SiFive RISC-V cores
- ARM Cores
- ARM Mail GPU
- Synopsys/ARC
- Imagination
- Cadence/Tensilica
- CEVA DSP
- Custom AI Accelerators

Standard Cell Libraries

- ARM/Artisan
- TSMC
- Synopsys/Virage
- Dolphin
- High Performance Kits

Memories

- SRAM (HS, HD, UHD, LP)
- Register Files
- ROM (Metal/VIA/Diff)
- Efuse
- ECC and Repair
- CAM/TCAM
- 1T-SRAM
- OTP/MTP
- eflash

Specialty IO's

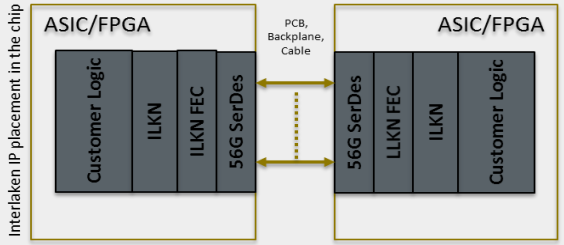
- LPDDR5/4
- DDR4/3
- GDDR6
- LVDS
- HSTL 1.8/1.5
- QDR
- SSTL-2/18/15
- PCI, PCI-X 1.0
- PCI-X 2.0
- USB 1.1
- GMII/RGMII
- PECL
- CML
- I^2C
- I3C
- Multi-voltage
- Oscillator IO
- MFIO (LVCMOS, SSTL, HSTL)

Differentiated IP Solutions

Interlaken IP Subsystem

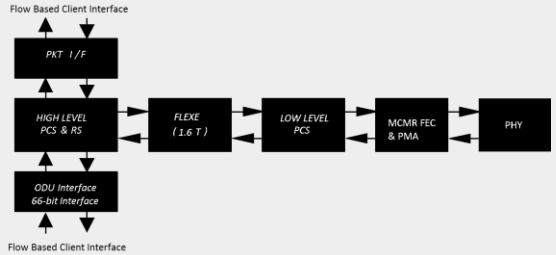
ILKN & ILKN FEC

- #1 Provider in market
- 75+ IP licenses
- Works with up to 48 parallel physical SerDes lanes 3.125 Gbps to 112 Gbps speeds
- Supports bandwidth of up to 1.2 Tbps



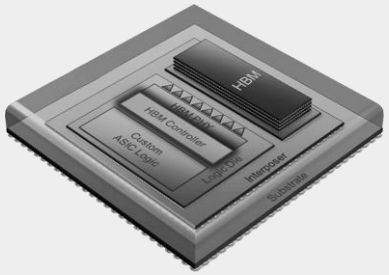
Ethernet IP Subsystem

- **400/200/100/50/25GbE** MAC+ PCS+ FEC IP
- Integrated with various SerDes in 16nm and 7nm
- Flex IP for Optical Transport market



High Bandwidth Memory (HBM) IP Subsystem

- IP subsystem solution (**Controller + PHY+ I/O**)
- HBM2 IP availability since Q4 2015
- Silicon Proven IP
- IP available in **22FDx, 16nm, 14nm and 7nm**
- Received Customers' Choice Award for best paper at TSMC NA OIP 2017

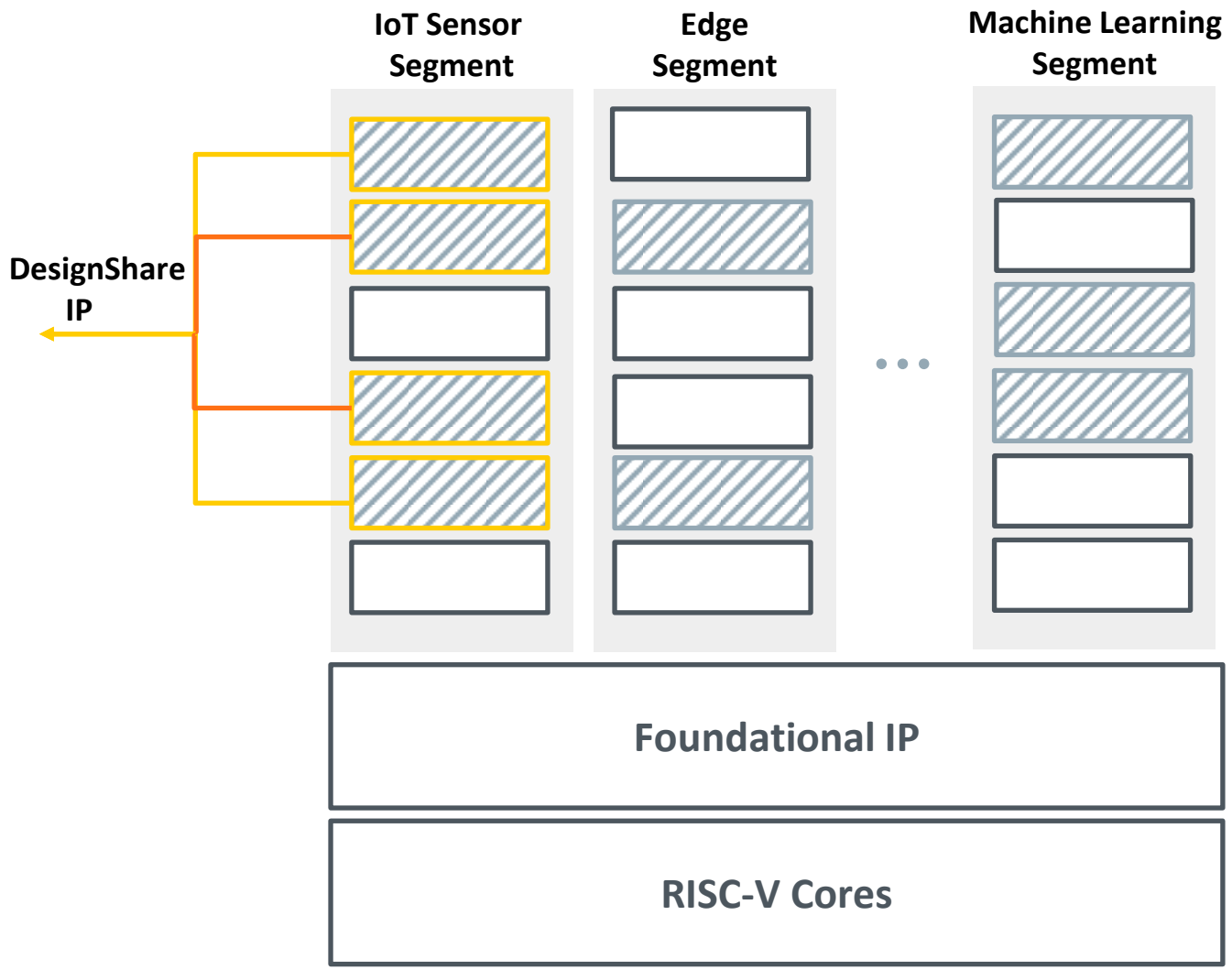


DesignShare Dramatically Reduces Prototyping IP Costs to ZERO

- DesignShare Partners provide their IP for SiFive Freedom Platform at **zero** cost

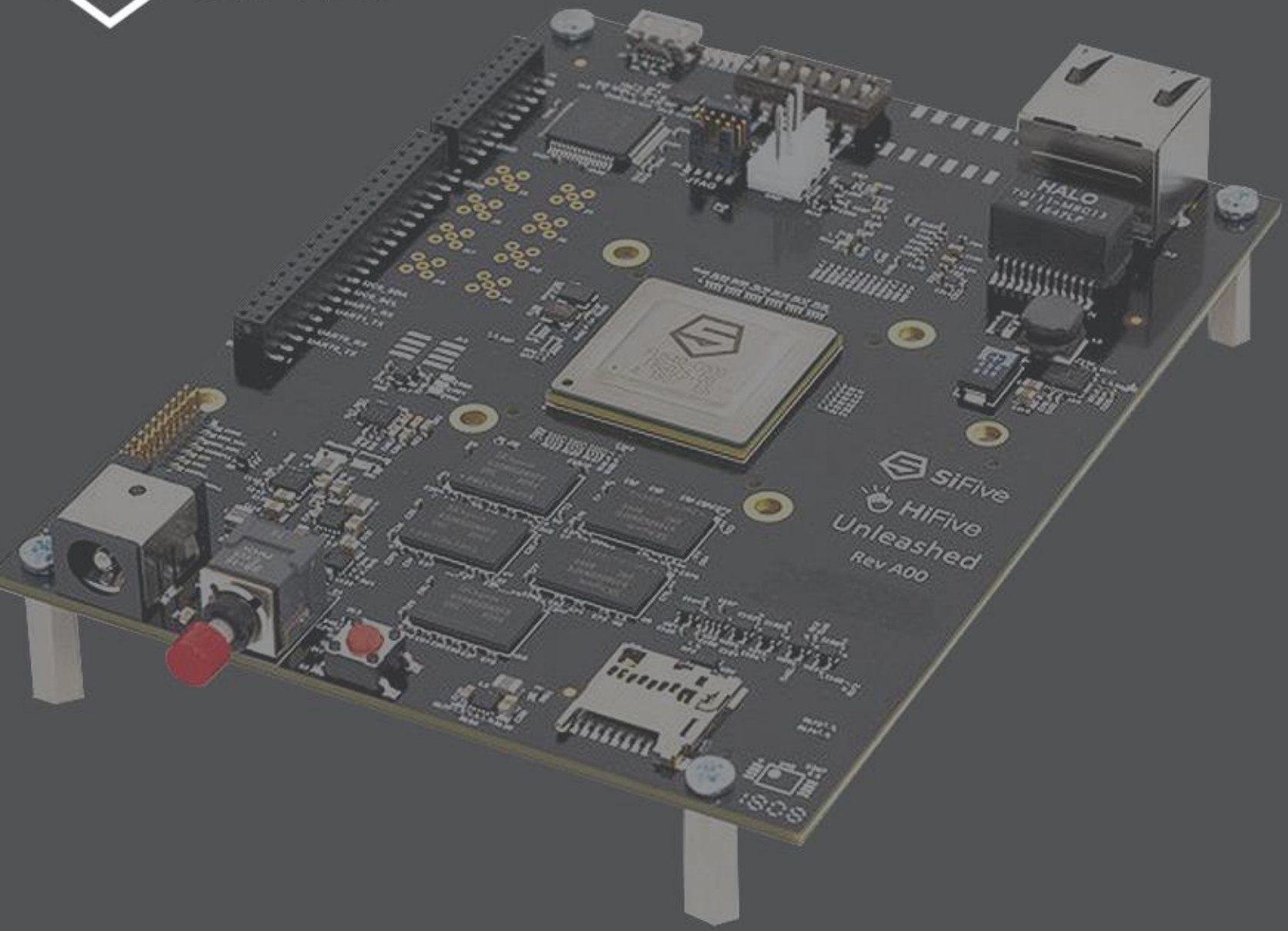
- Benefit to DesignShare Partners
  - Dramatically increase number of design starts
  - IP Protection via SiFive
  - SiFive collects NRE/Royalties in production and provides to partners

- Benefits to Customers
  - Reduces expertise needed
  - Single contract/NDA



Growing DesignShare Community – Come Join Us!

SiFive



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