SiFive 推动垂直领域技术创新

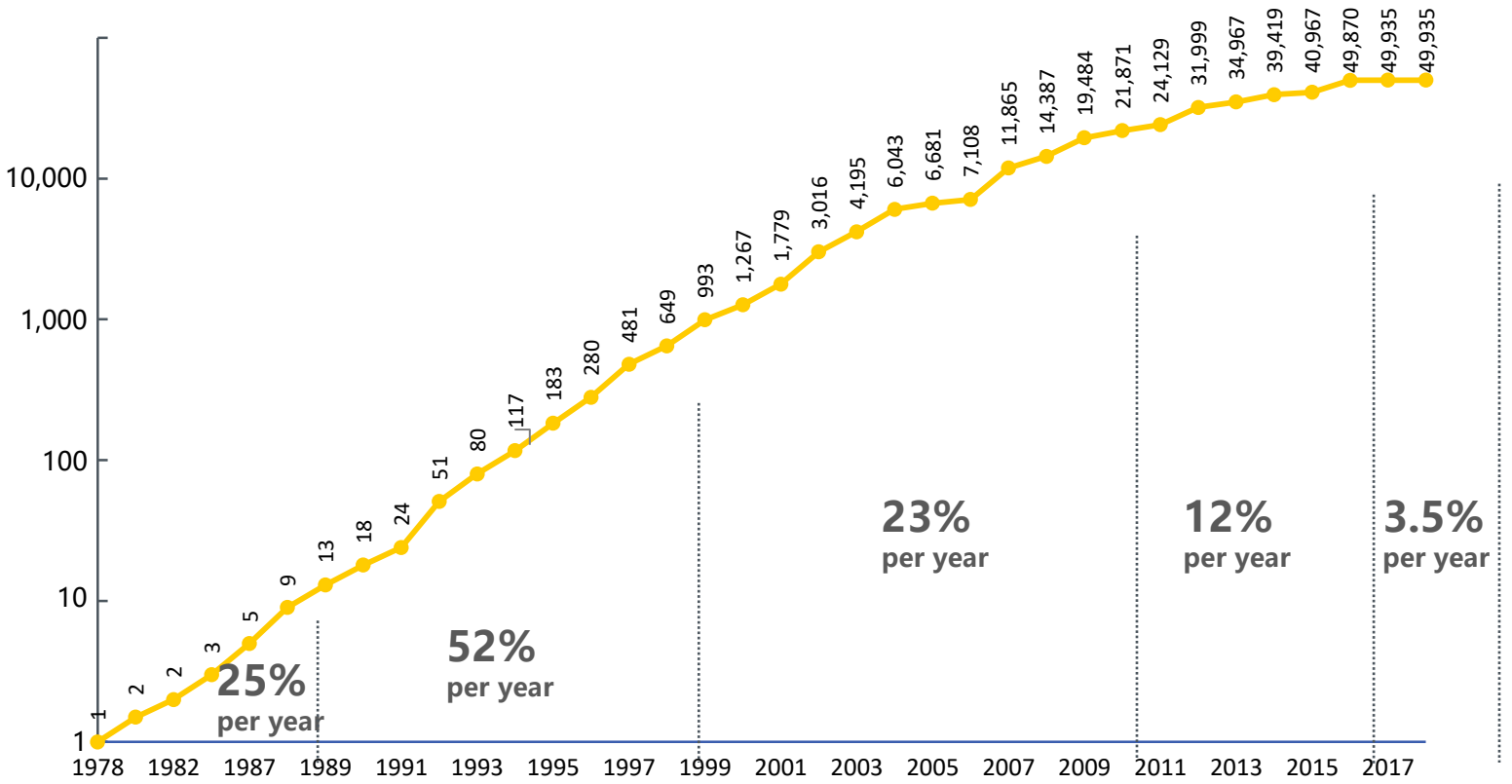
Promotes Technological Innovation in Vertical Domain

Jun. 2019

后摩尔时代的机会

Moore's law is SLOWING DOWN

General-purpose CPU performance (vs. VAX-11/780)



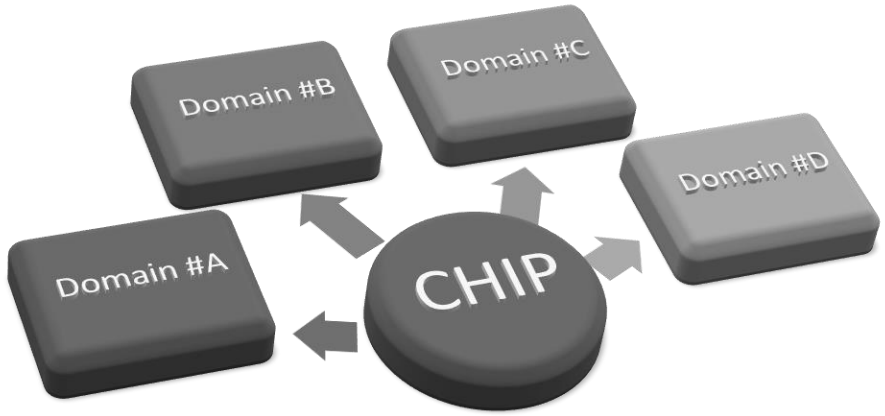
More Than Moore

- *Hardware Efficiency*
- *Architecture Innovation*
- *Application Driven*

Chip Should be Customized

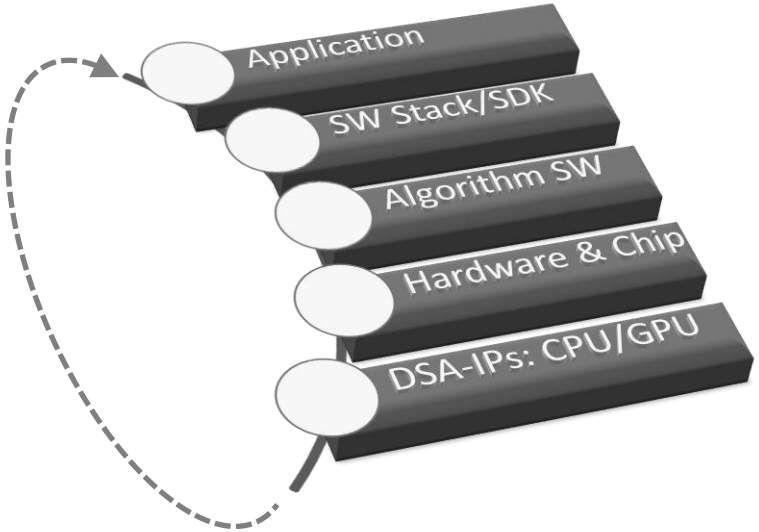
两种不同的创新模式

Chip Company mode: *Qualcomm*



- **Chip First, then System**
- **Software depend on hardware resource**
- **Chips Drive the technological innovation**

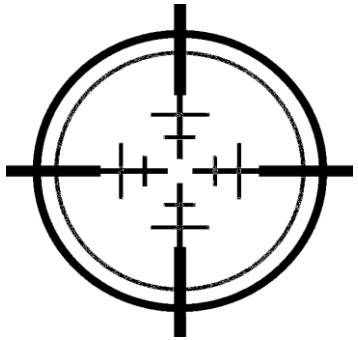
Vertical Customization mode：*Apple*



- **Application scene → algorithm**
- **Software definition chip**
- **Application is the driving force of tech. innovation**

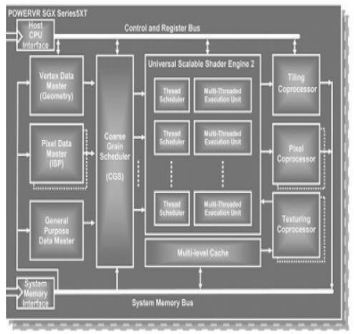
…… Chip Customization in Vertical Domain is the future

垂直定义模式的特点



Focus
目标专注

One chip-spec for one application scenarios, Domain-related knowhow



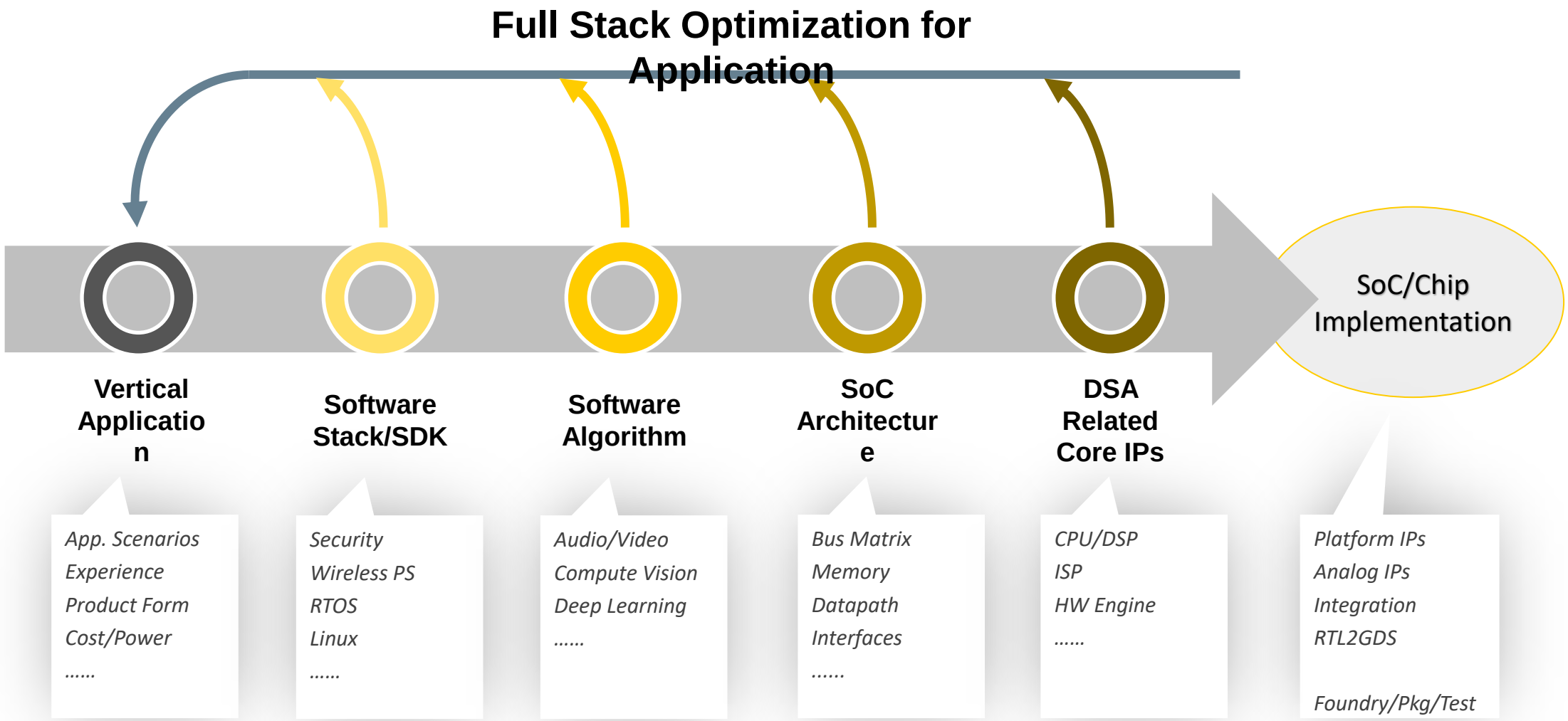
DSA Hardware
独有硬件

Unique Chip with DS Architecture builds the core Competence

Optimization
全栈优化

Full Stack Optimization *enhances the overall competitiveness*

从应用到芯片的全栈优化

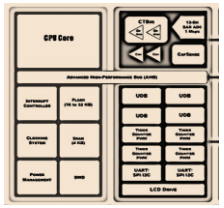


挑战

Challenge……

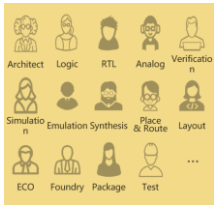
IP Resource

Flexible IPs for DSA



Platform

SoC infrastructure



Team

More than 14+ Disciplines

Time

Long time to get silicon for validation

Cost

3rd IPs License, MPW, package for Verify

Help from SiFive……

SiFive提供的RISC-V CPU内核的技术特点

1. RISC-V CPU Core

Only RISC-V **Standard** ISA

2. Max Configuration

Scalable & Modular Design

3. Continue Open

Open Source Projects

多个系列的成熟CPU内核IP

SiFive RISC-V IP Series

E Cores | S Cores

Industry-leading 32-bit/64-bit Embedded cores

7 Series High Performance	Storage Networking Automotive	S76, S76-MC E76, E76-MC
3/5 Series Power Efficiency	Industrial Modems Storage	S51, S54 E31, E34
2 Series Power Consumption	Microcontrollers IoT Wearables	E21, E24 E20

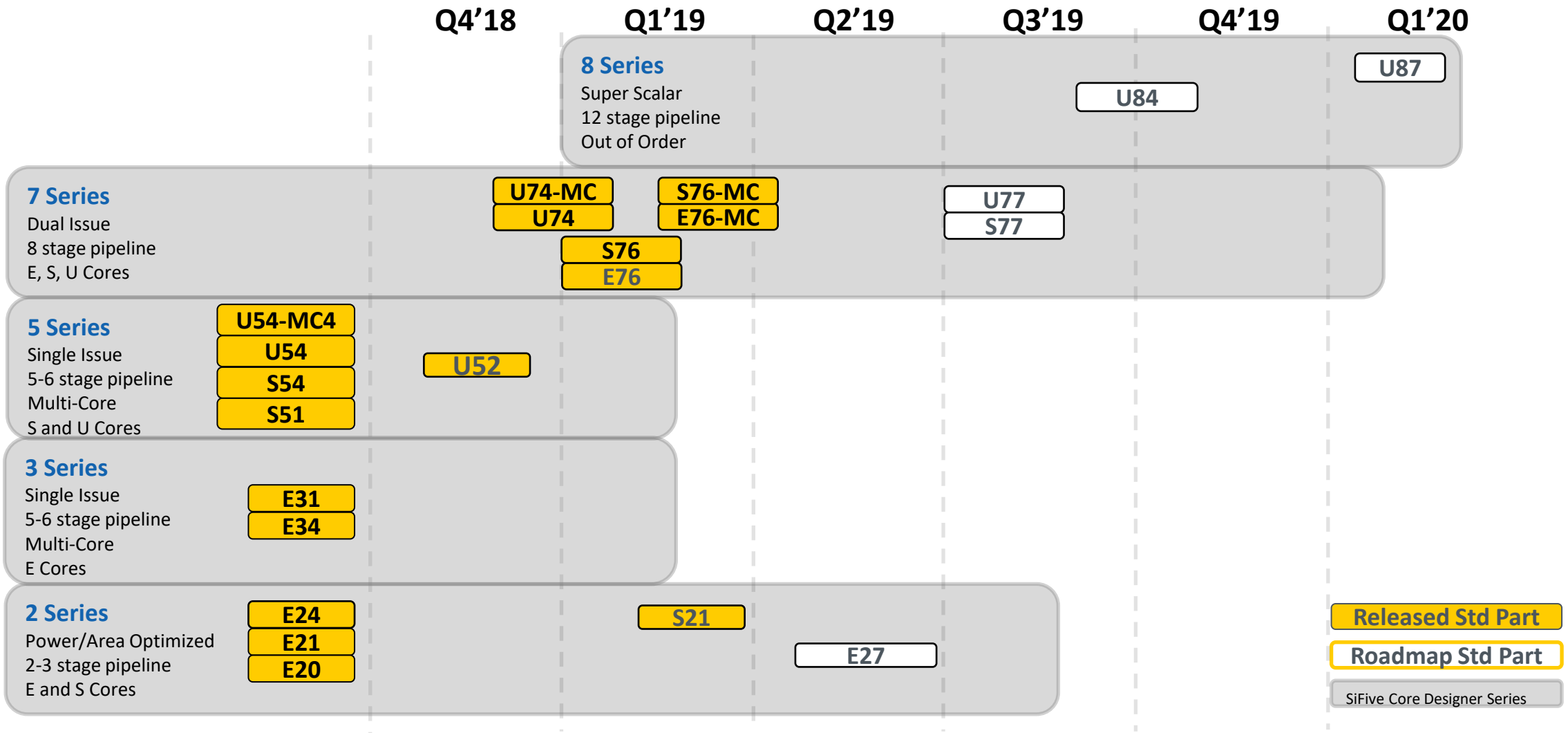
U Cores

High performance 64-bit Application Cores

7 Series Highest Performance Multi-core for Linux	SBC Networking Consumer	U74 U74-MC
5 Series Multi-core for Linux	Low Cost Linux Industrial Gateways	U54-MC U54

--- All CPU cores support configurable features According to DSA ideas

更多高端内核IP即将推出

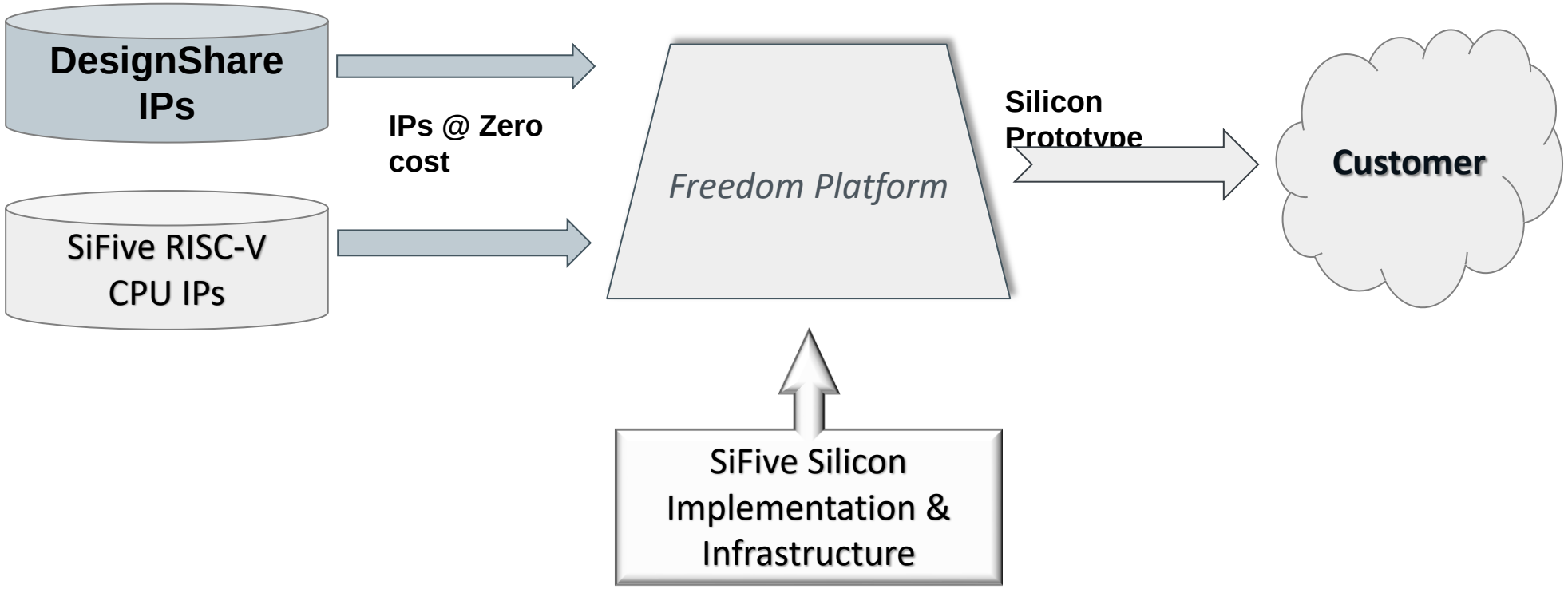


--- continue to be the leader the risc-v technology

支持多种内核的在线定制

--- Design your own CPU core within 1 hour

DesignShare ➔ 全力打造的技术创新环境



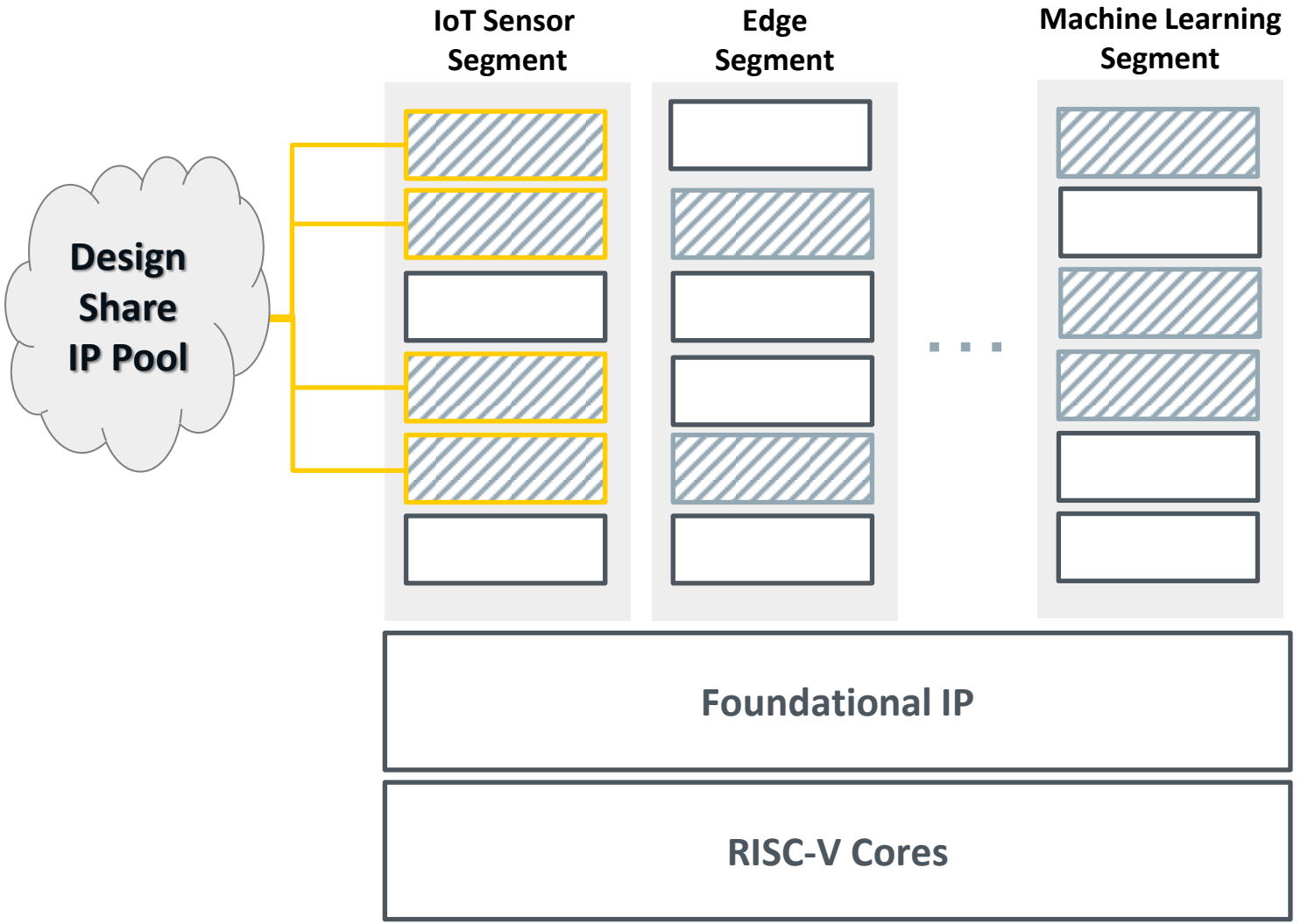
--- Lowest Cost for Innovation Verify

DesignShare推动IP与SoC联动发展

- *Partners provide their IP for SiFive Freedom Platform at* ***zero*** *cost*

- *Benefit to Partners*
  - *Increase design starts*
  - *IP Protection via SiFive*
  - *SiFive collects NRE/Royalties in production and provides to partners*

- *Benefits to Customers*
  - *Reduces expertise needed*
  - *Single contract/NDA*



越来越多的DesignShare合作伙伴

DesignShare现有IP资源

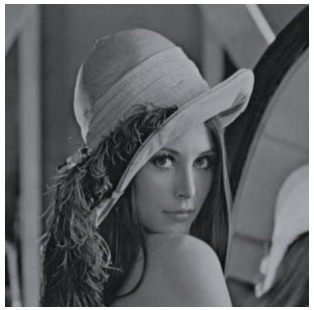
☑ DesignShare Partner

Features/IPs	IP Type	IoT	AR, VR, Surveillance	Edge Inference
Process Node	**-**	**Low Power Node**	**FinFet Node**	**FinFet Node**
Main Processor	**Soft IP**	E2/3 Series	U7 Series	U7-MC Series
Control Plane/Micro Controller	**Soft IP**	E21	E27	S71
Memory Controller	**Soft IP**	N/A	☑ (LPDDR4)	☑ (LPDDR4)
Memory PHY	**Hard IP**	N/A	☑ (LPDDR4)	☑ (LPDDR4)
System Bus	**Soft IP**	AXI/TileLink	AXI/TileLink	Tilelink
Embedded FPGA	**Hard IP**	☑ ☑	N/A	N/A
AI / DLA	**Soft IP**	☑ , Customer Specific	☑, Customer Specific	☑, Customer Specific
L2 Cache	**Hard IP**	None	2MB Shared	2MB shared with System
Video Encoder	**Soft IP**	None	☑ H264/H265	☑ H264/H265/VP9
Video Decoder	**Soft IP**	None	☑ H264/H265	☑ H264/H265/VP9
Audio Interface	**Soft IP**	4x PDM, 4x I2S, 4x ANA	I2S/TDM/PDM	None
USB PHY	**Hard IP**	N/A	☑ (1x USB 3.1, 1x USB2.0 Host)	N/A
USB Controller	**Soft IP**	N/A	☑ (1x USB 3.1, 1x USB2.0 Host)	N/A
Ethernet Controller	**Hard IP**	N/A	☑ (10GbE)	☑ (100GbE)
Ethernet PHY	**Soft IP**	N/A	☑ (10GbE)	☑ (100GbE)
Camera Interface	**Hard IP**	☑ (LVDS,MIPI)	☑ (2x CSI-4)	None
GPU	**Soft IP**	☑ (2D)	☑ (2D, 3D)	None
Storage Interface	**Hard IP**	None	☑ (SD 4.0, UHS-1, eMMC 5.1)	None
PCIe Controller	**Soft IP**	None	☑ (PCIe Gen4)	☑ (PCIe Gen4)
PCIe PHY	**Hard IP**	None	☑ (PCIe Gen4)	☑ (PCIe Gen4)
ADC/DAC	**Hard IP**	☑ (12bit ADC, 12 bit DAC)	☑ (12bit ADC, 12 bit DAC)	N/A
Security	**Soft IP**	☑ AES/SHA Sec Boot	☑ Root of Trust, Secure Boot, Crypto	☑ Root of Trust, Secure Boot, Crypto
GPIOs, PLLs, efuse, Std cells	**Hard IP**	☑	☑	☑
Peripherals	**Soft IP**	☑ (I2C, UART, WDT, SPI, I2S, RTC)	☑ (I2C, UART, WDT, SPI, I2S, RTC)	☑ (I2C, UART, WDT, SPI, I2S, RTC)

更多的IP资源正在加入DesignShare

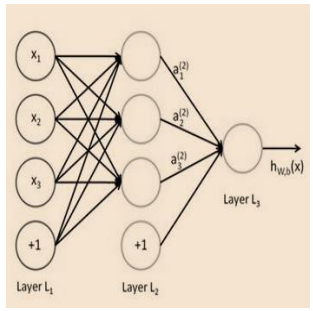
DSP

Voice/Vision



ISP

Image Processor for AI



NPU

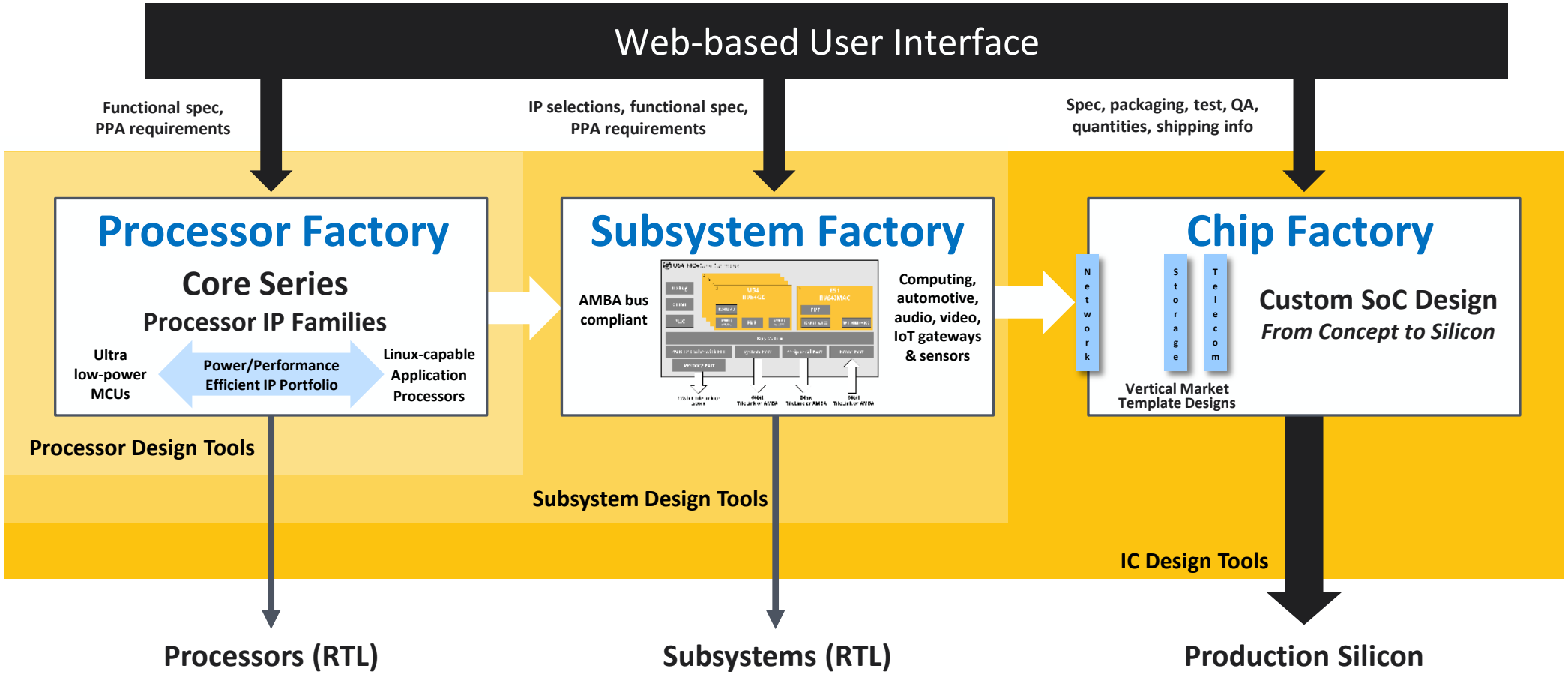
Neural Processor

PMU

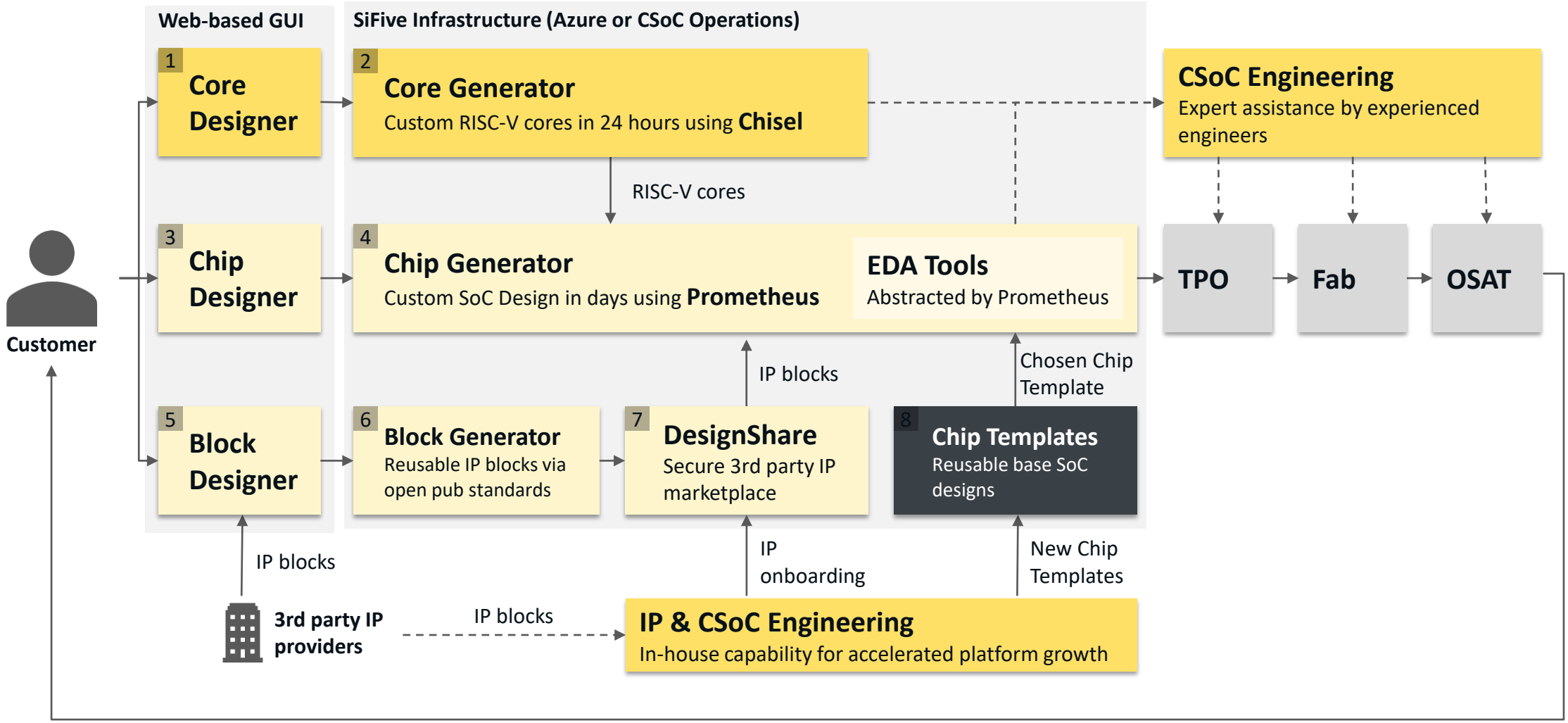
Low Power PMU

--- Focus on New requirement of AI IoT

云端设计环境 ➔最高效的设计思想反馈

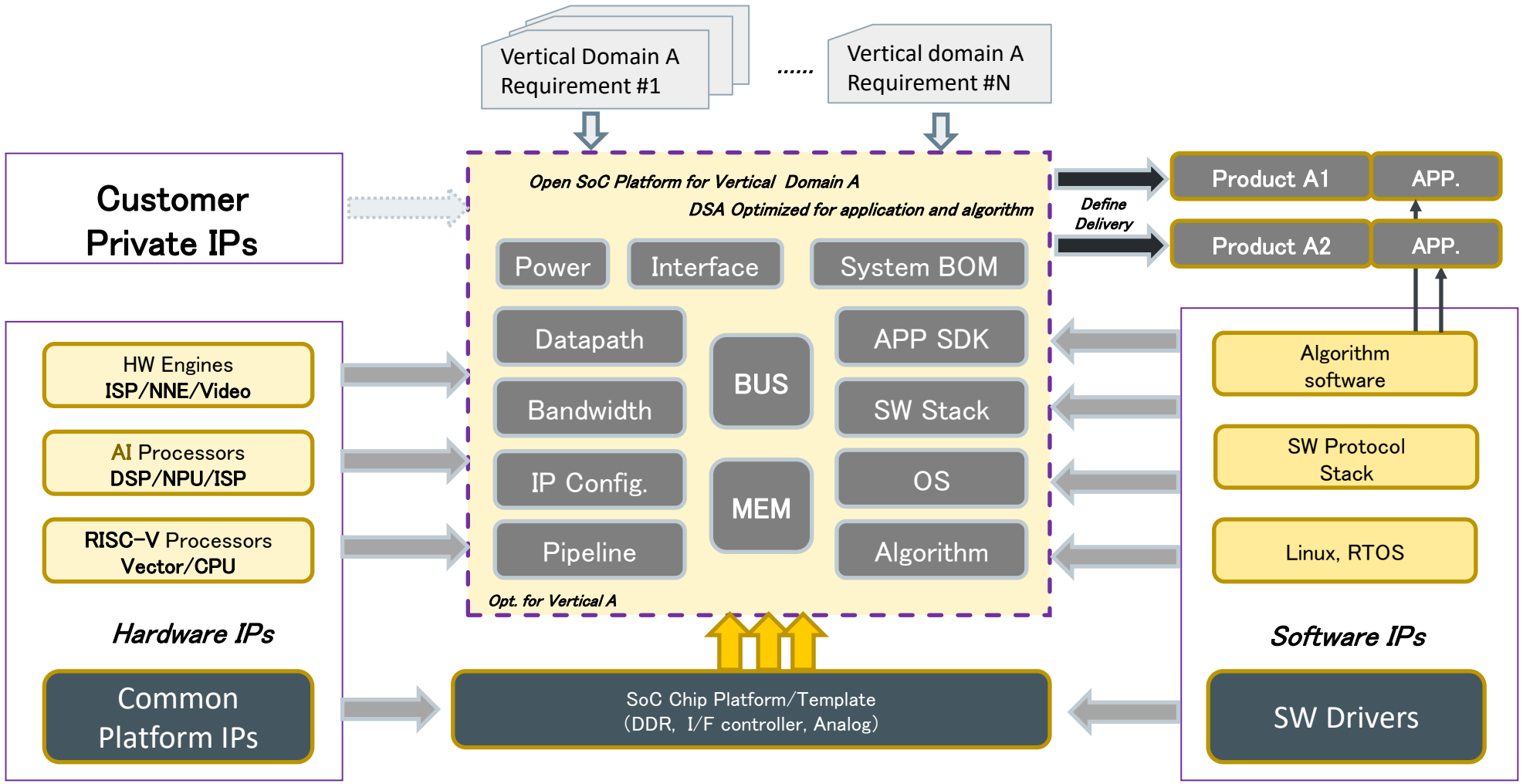


敏捷设计能力➔创新成果的快速交付



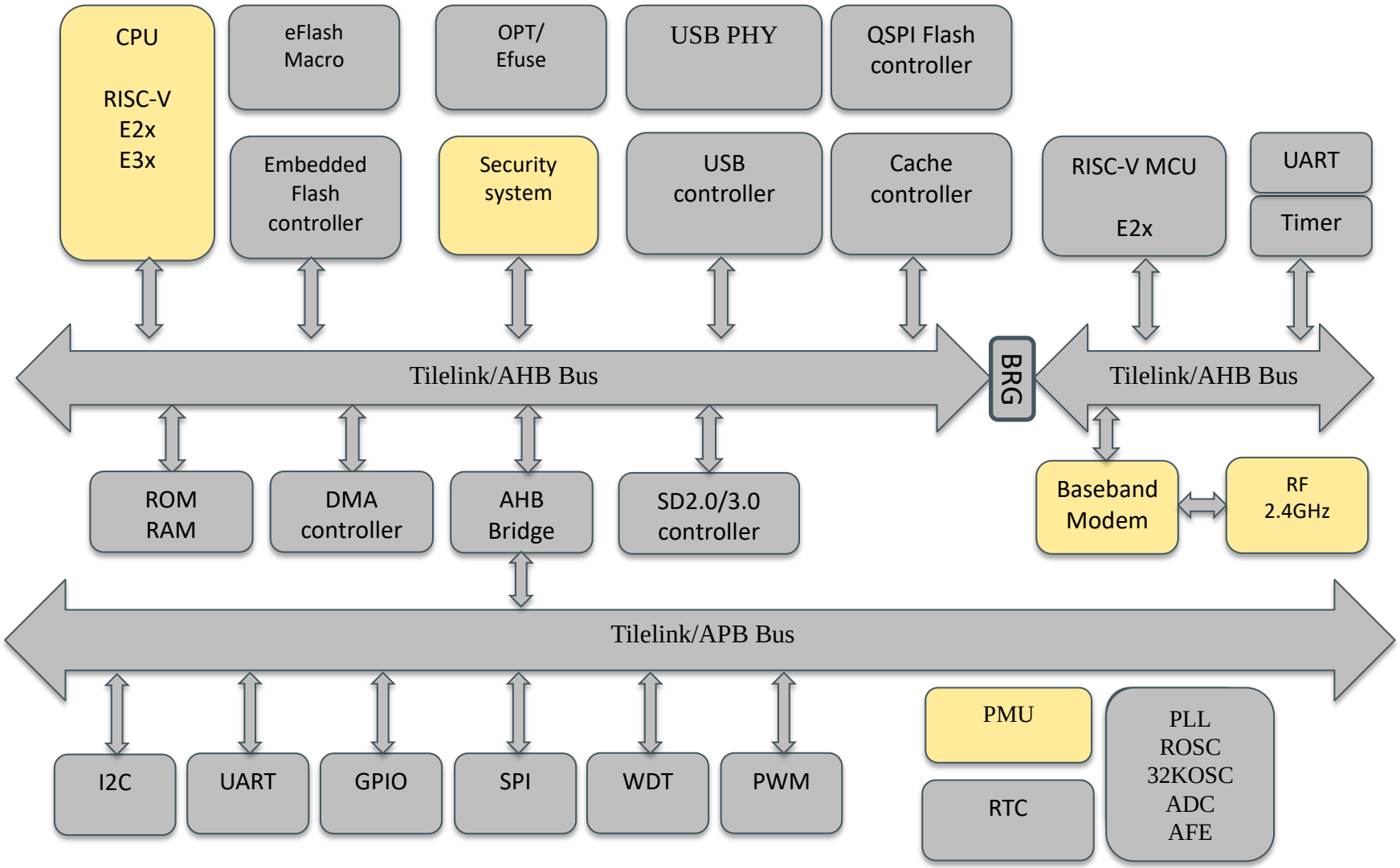
…… Custom SoC delivered in 12 weeks

DSA SoC平台模板➔ 垂直领域的创新加速器



针对垂直领域应用优化的DSA SoC platform(Template)

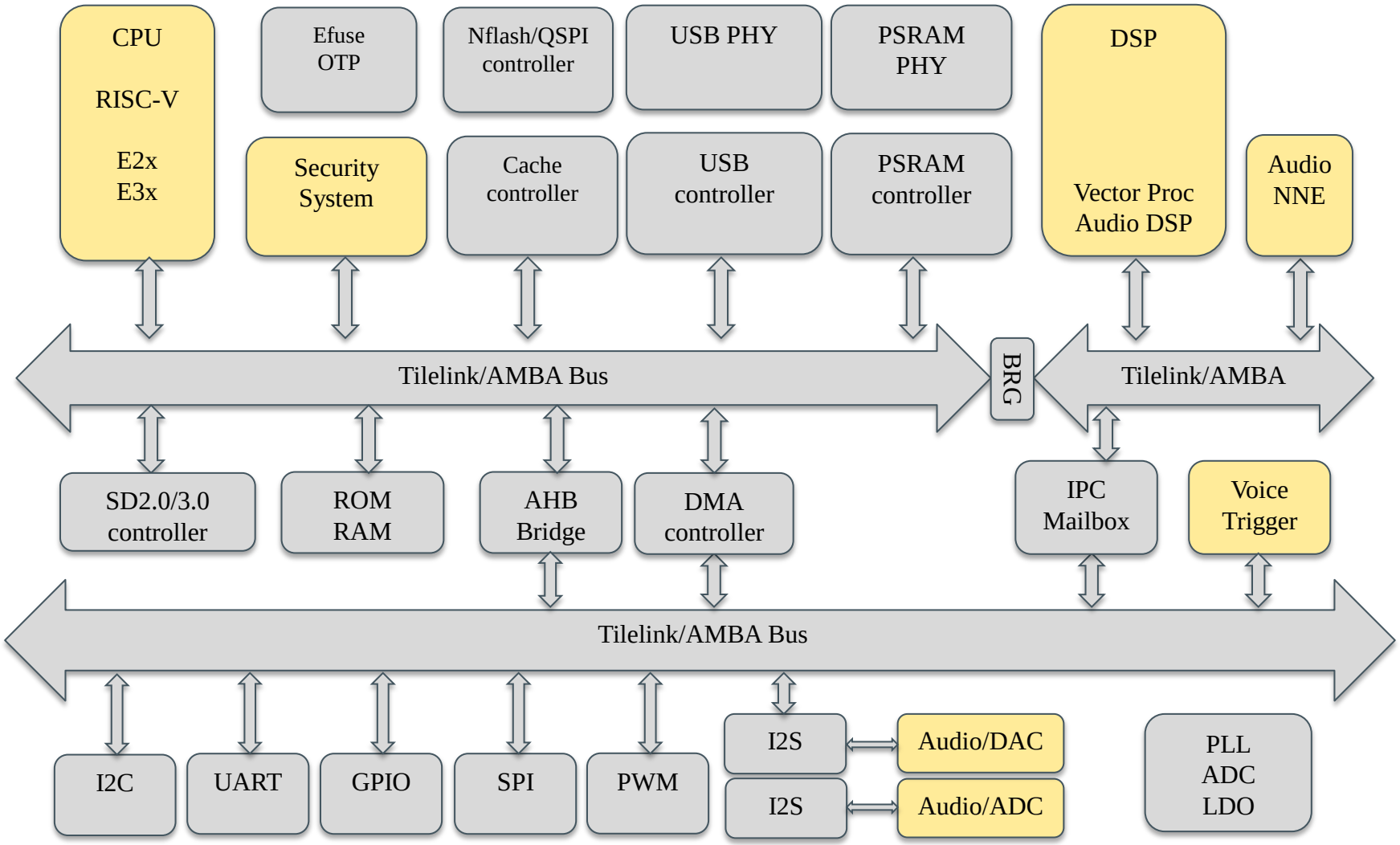
Template典型案例 – 1 （IoT-MCU）



《平台价值》

- 超低功耗
- 安全方案
- 成熟SDK
- 更低成本
- 无线连接

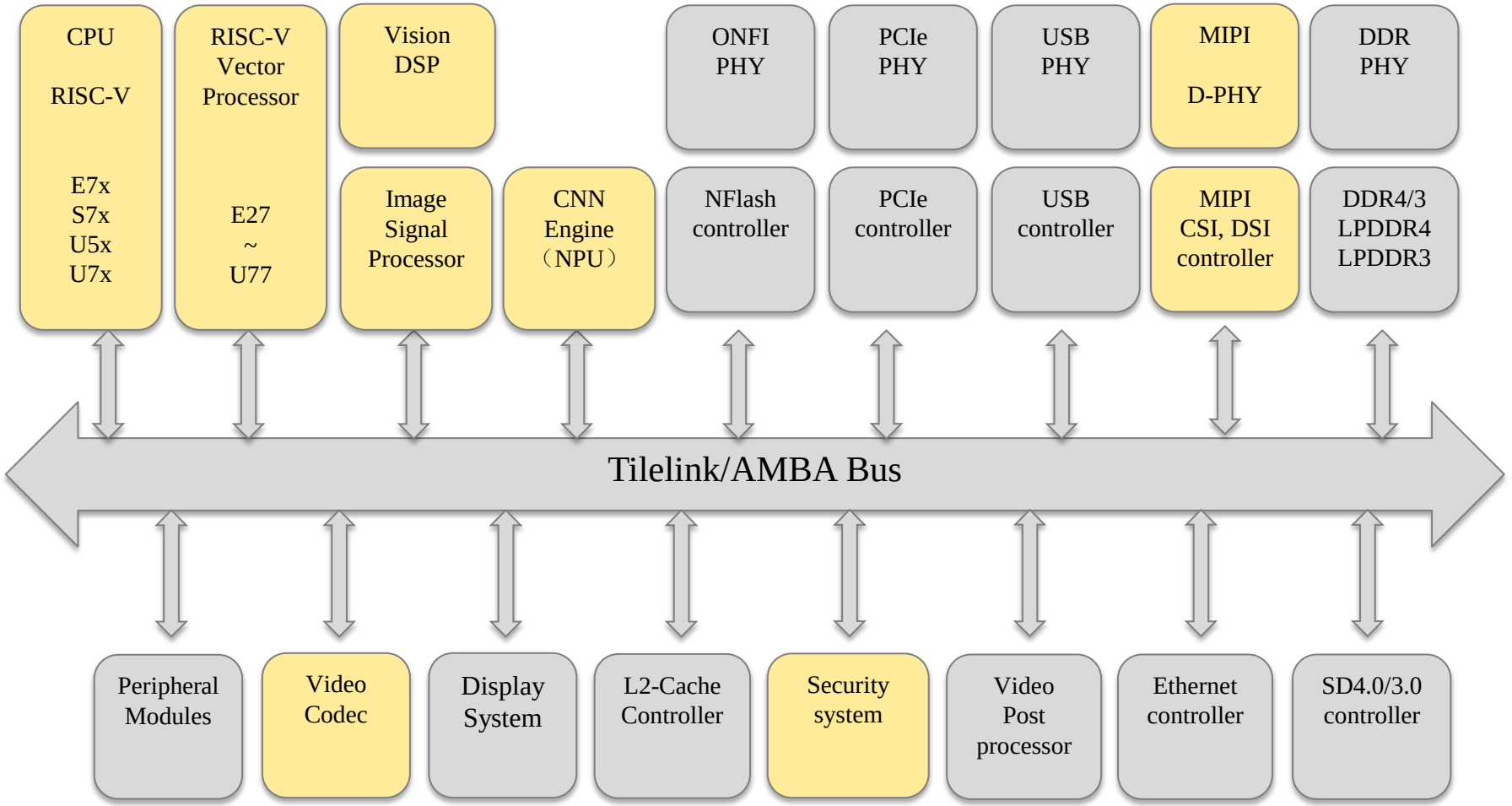
Template典型案例 – 2 （Smart Audio）



《平台价值》

- 低功耗
- 音频算法
- 智能算法
- 低成本
- 安全方案

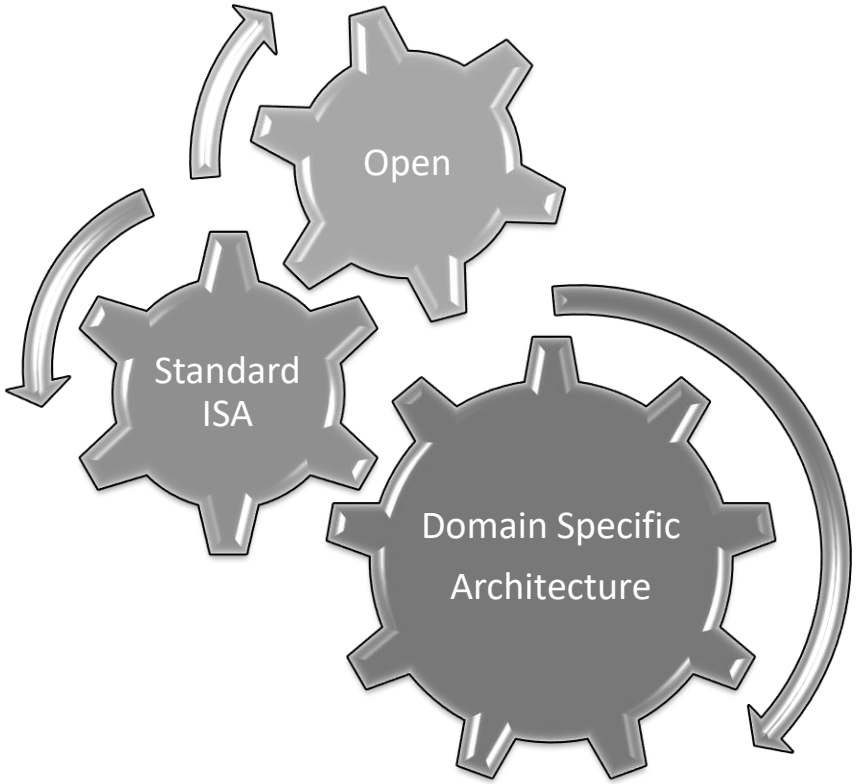
Template典型案例 – 3 （Smart Video）



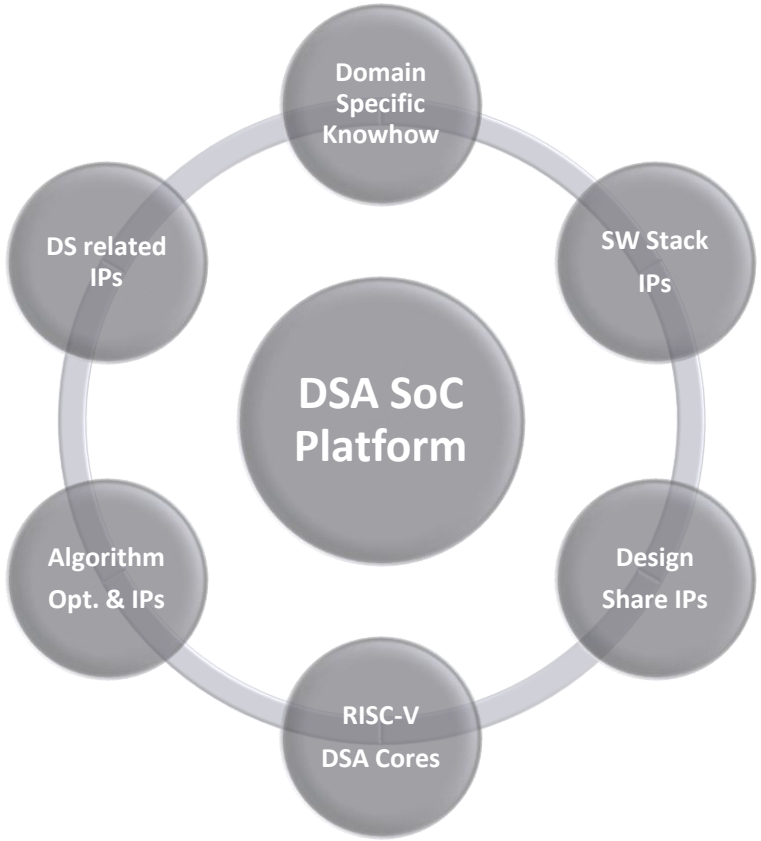
《平台价值》

- 计算能效
- 视频处理
- 视觉算法
- 深度学习
- 可靠计算

SiFive ←→ DSA Innovation



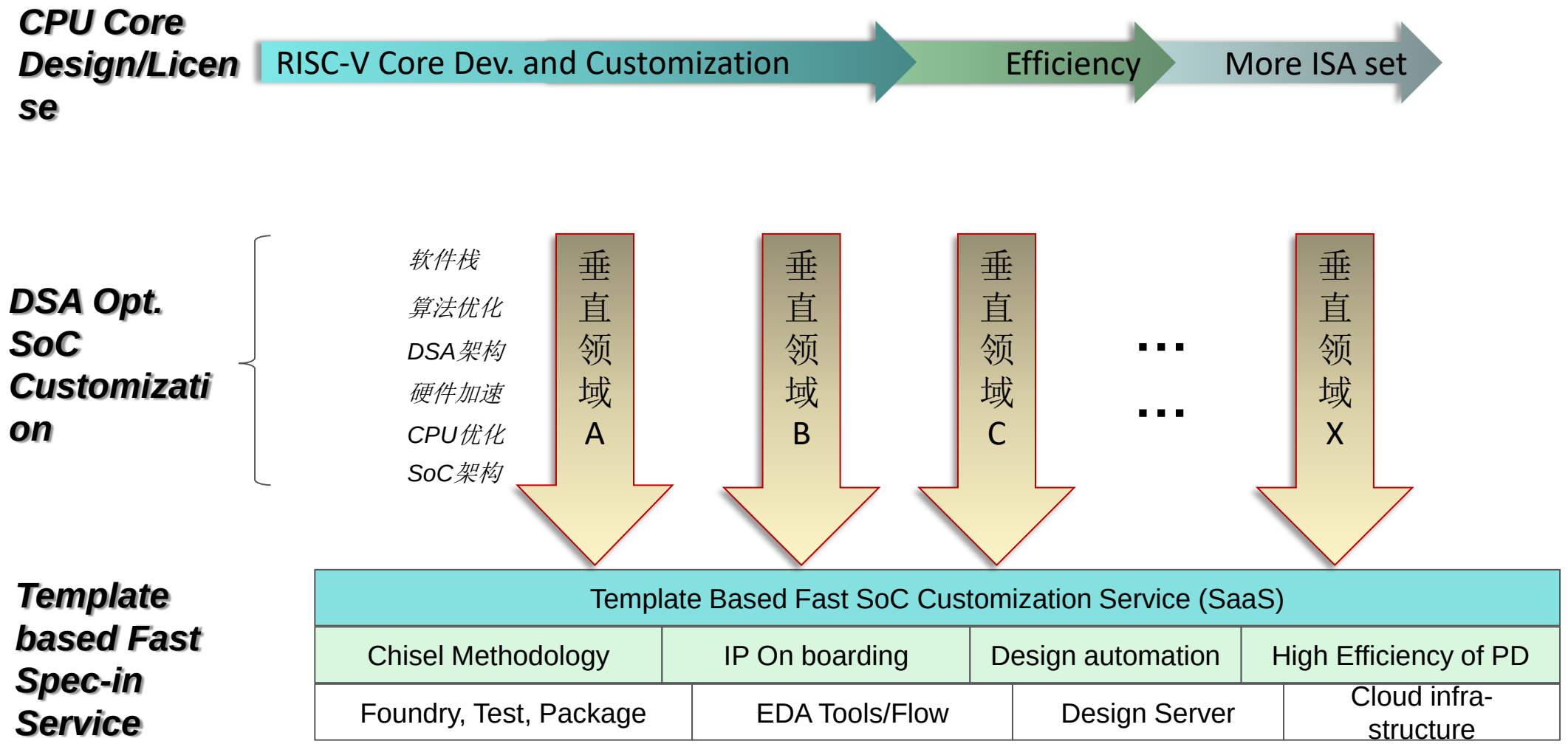
DSA



Better RISC-V CPU Core

Continue Innovation of SoC Arch and solution

SiFive Valuable Technology Structure



DSA Innovation Together!