CHISEL: CHIP INDUSTRY REFACTORING FOR AI

Liwei.Ma@Sifive.com

Sifive China

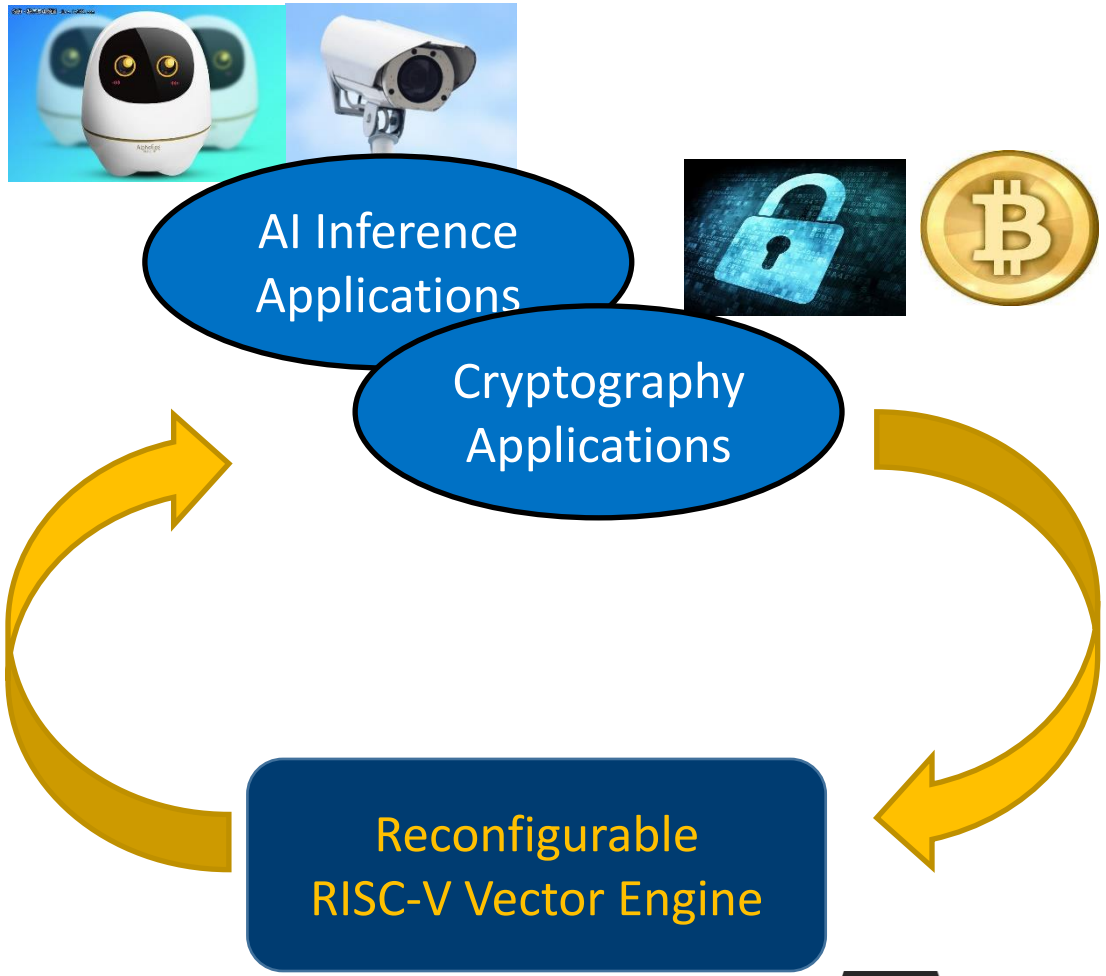
Outline

- Call for broad collaborations to address new challenges
  - Collaboration across entities
  - Contribution to new technologies
- An AI revolution for chip industry
  - A gap between IoT AI market and chip industry
  - Hardware agile design across full industry chain
- Sifive solutions for technology democratization
  - Chisel and diplomacy for agile hardware design
  - Wit/Wake for agile SoC integration

SiFive

Collaboration across Industry Chain

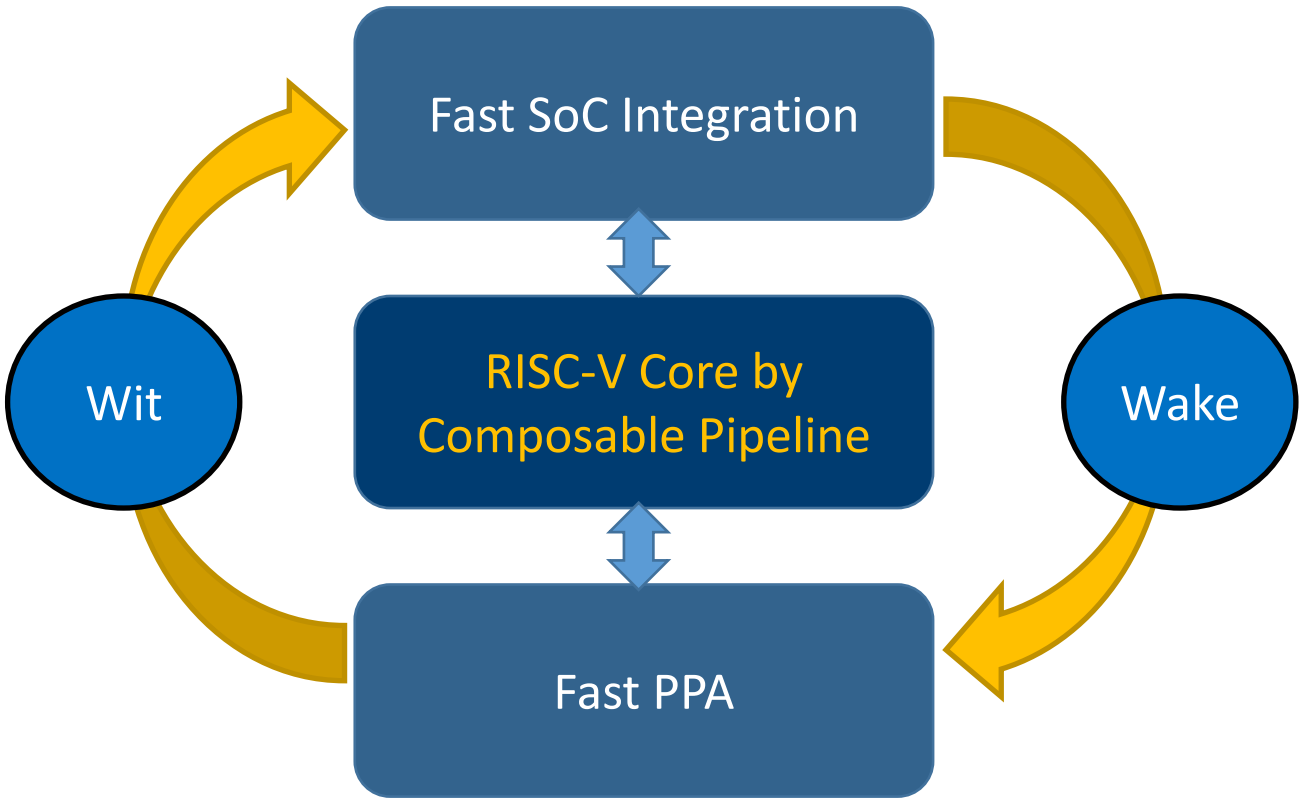
- Sifive China ALL IN RISC-V vector for AI
- Engage with customers for fast feedback loop
  - Hardware agile design
- Focus on technologies that matter
  - AI inference
  - Encryption



SiFive

Contribution to New Technologies

- Sifive China ALL IN Chisel/Wake agile development technologies
  - Origin from Berkeley and spirit of Sifive
- Engage with Tech Geeks
  - Rebuild tech aesthetics
- Focus on problems
  - What design, verification and integration truly are



SiFive

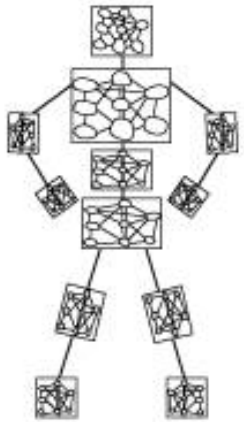
Outline

- Call for broad collaboration to address new challenges
  - Collaboration across entities
  - Contribution to new technologies
- An AI revolution for chip industry
  - A gap between IoT AI market and chip industry
  - Hardware agile design across full industry chain
- Sifive solutions for technology democratization
  - Chisel and diplomacy for agile hardware design
  - Wit/Wake for agile SoC integration

SiFive

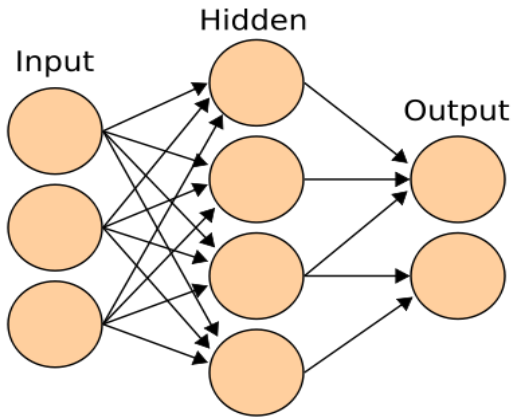
Three Pillars and Steps of AI

Symbolism



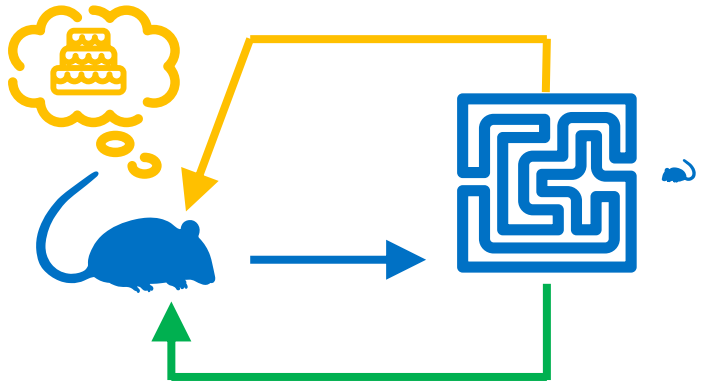
Programming by experts

Connectionism



Programming by everyman

Behaviorism



Programming by machine

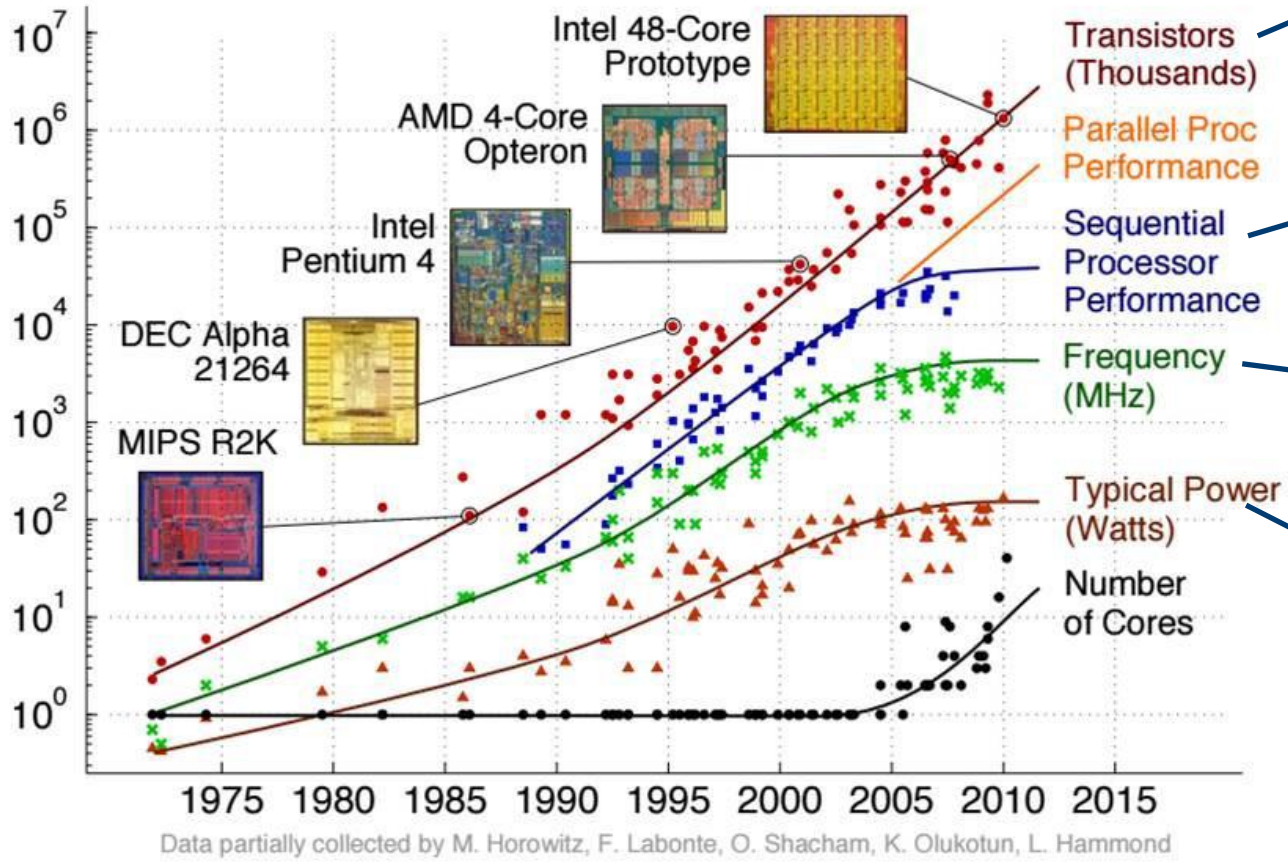
SiFive

Three Waves of General Purpose Computing

PC era	Mobile internet	Internet of things
Discrete device	Chip is a system	System defines chip
CPU+ASIC	SoC	Integrated service
Symbolism	Symbolism	Connectionism

SiFive

The End of Moore's Law



Feature size reaching physical limits

Linear pin number VS quadric area

Die size ≈ electronic wave length

Power density constant Dennard scaling law

SiFive

Fast Industry Chain at IoT AI

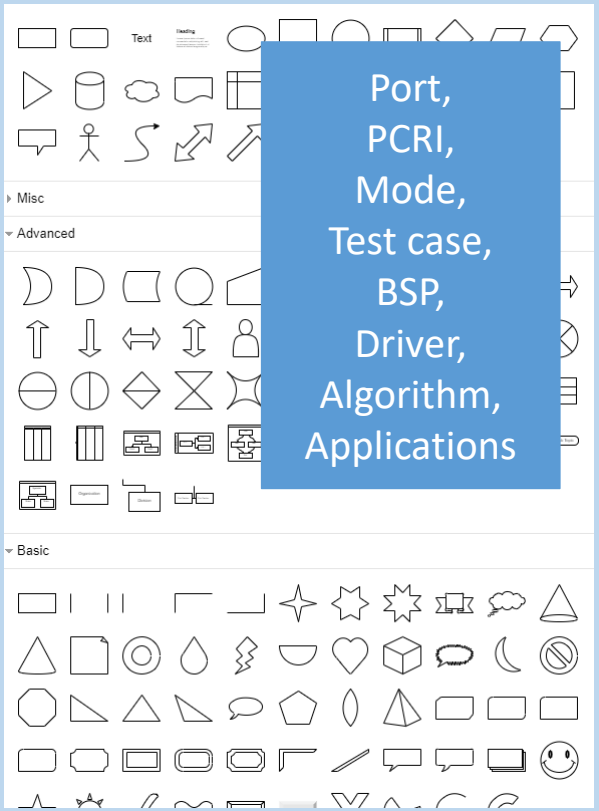
	Before	Now
Generation	18 months	9-12 months
Product form	Discrete devices	Integrated service
Software/hardware boundary	Clear	Hardware is soft Software as a service
Value chain	One-way from upstream to downstream	Two-way between upstream and downstream

Agile design is critical for chip industry

SiFive

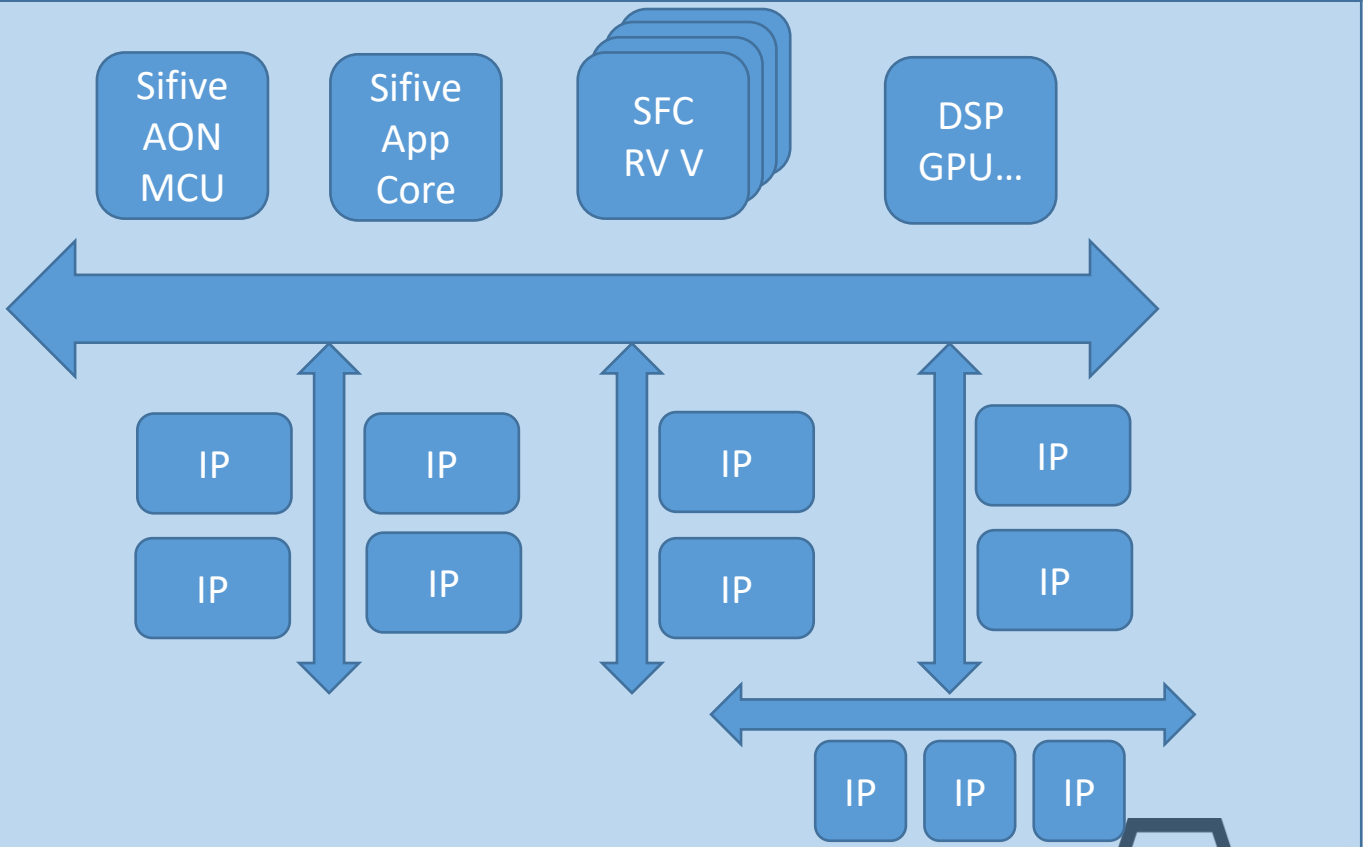
Fast SoC Integration with Standard IPs

IP Package Library



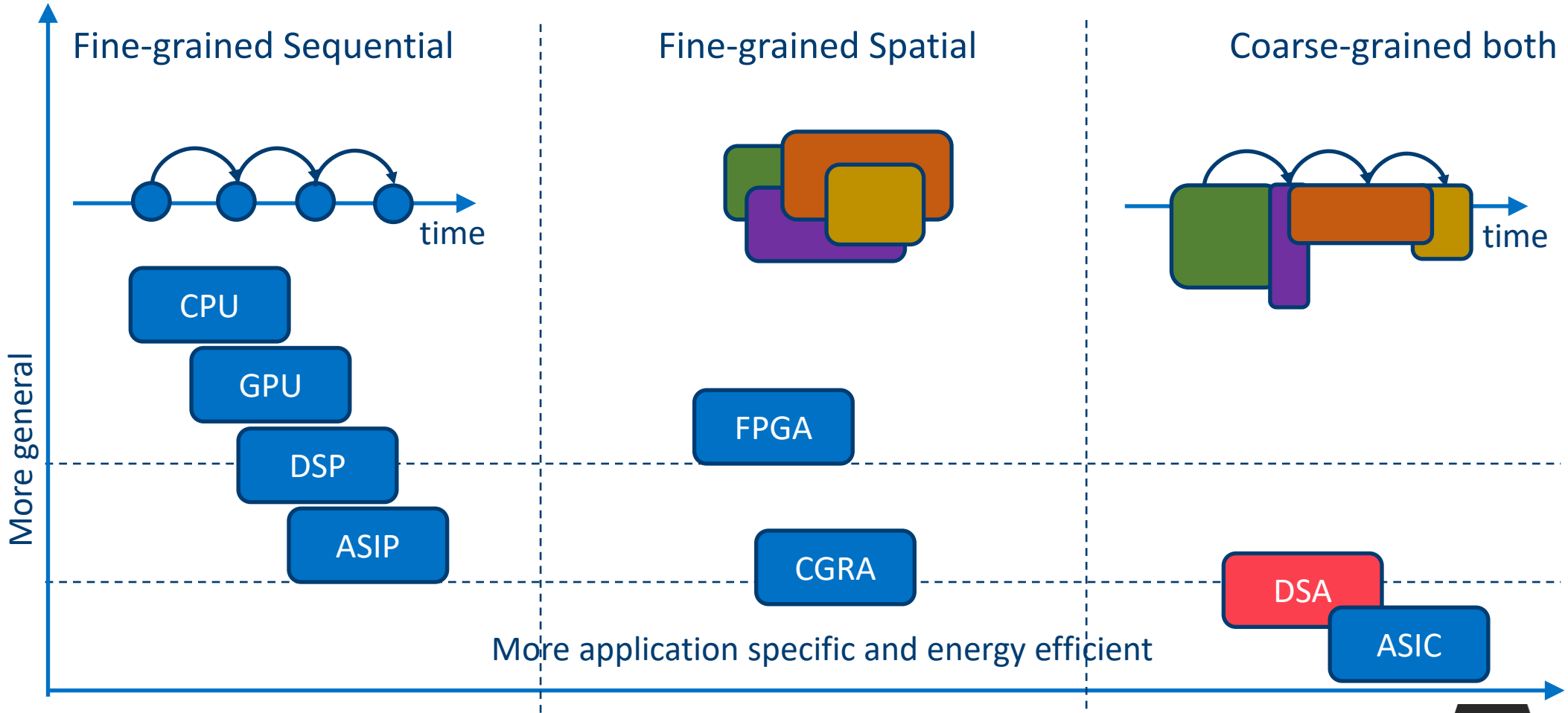
Port,
PCRI,
Mode,
Test case,
BSP,
Driver,
Algorithm,
Applications

SoC Integration Canvas (Web GUI or Scala Script)



SiFive

Fast Core Design as DSA



SiFive

Outline

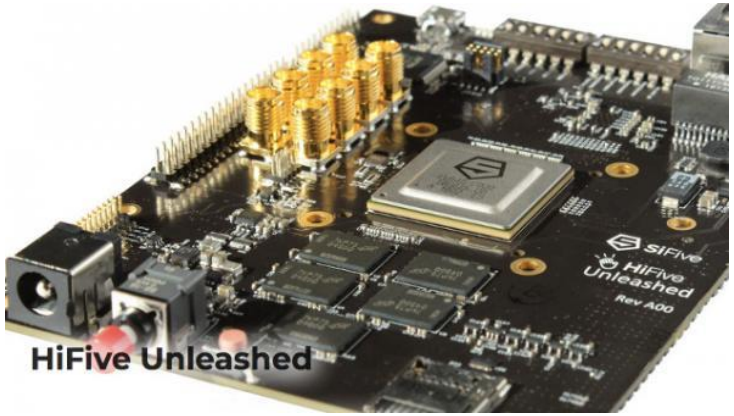
- Call for broad collaboration to address new challenges
  - Collaboration across entities
  - Contribution to new technologies
- An AI revolution for chip industry
  - A gap between IoT AI market and chip industry
  - Hardware agile design across full industry chain
- Sifive solutions for technology democratization
  - Chisel and diplomacy for agile hardware design
  - Wit/Wake for agile SoC integration

SiFive

To Present Design Options by Chisels

- Chisel
  - Constructing Hardware In Scala Embedded Language.
  - Not High-Level Synthesis
  - Domain-Specific Language for digital hardware design
  - Chisel is metaprogramming
- Describe circuit architecture
  - Chisel
- Describe circuit behavior:
  - Verilog, VHDL

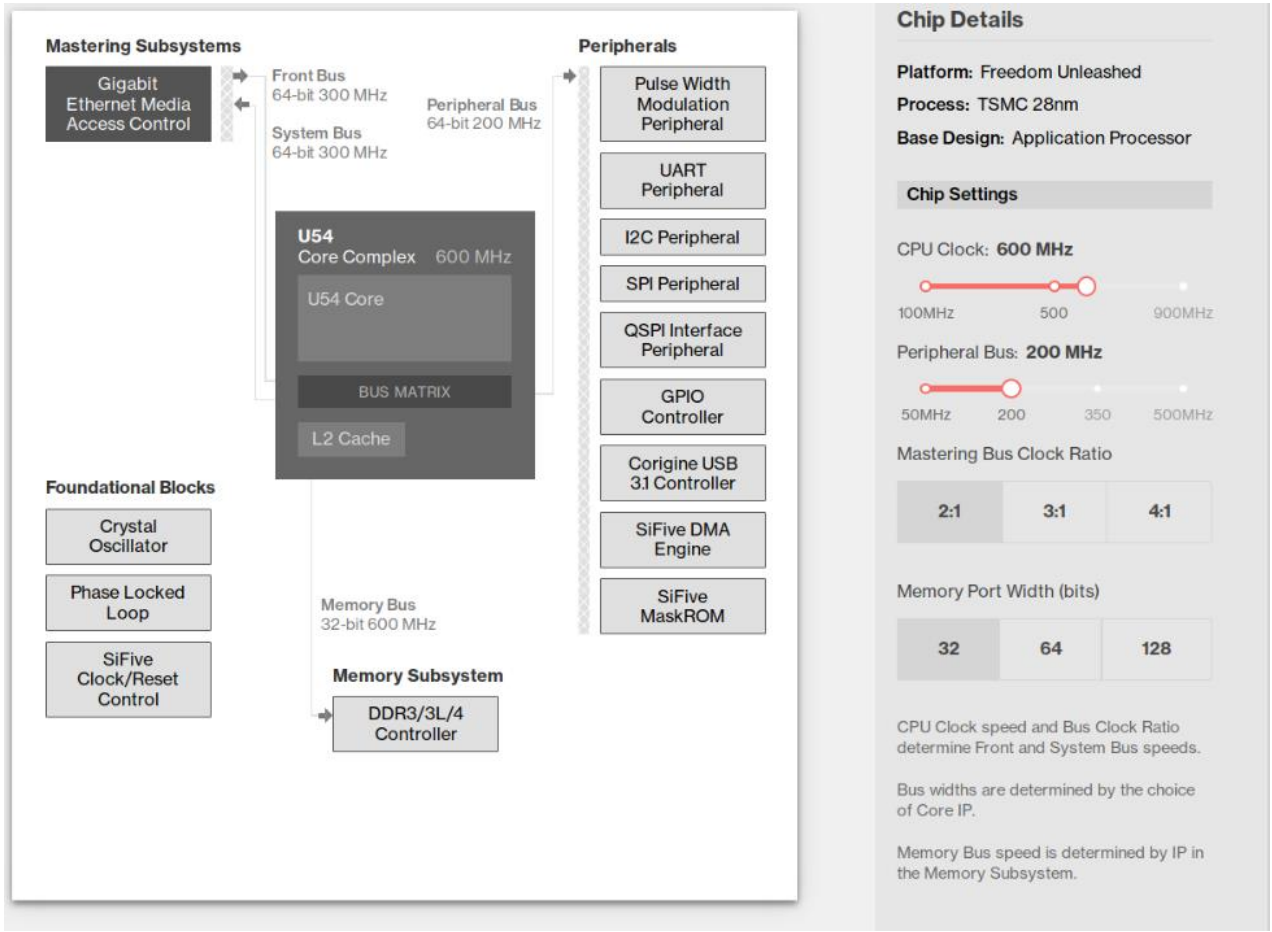
Chisels



Chips

SiFive

Optimize SoC Chip with Options (Chisel)



Chip

Chisel

SiFive

Learn More about Chisel 3

- https://chisel.eecs.berkeley.edu/chisel-getting-started-chinese.pdf

Chisel 3.0 Tutorial (Beta)

Jonathan Bachrach, Krste Asanović, John Wawrzynek
EECS Department, UC Berkeley
{jrb|krste|johnw}@eecs.berkeley.edu

Translator: Sand River
liwei.ma@gmail.com

May 8, 2017

1 引言

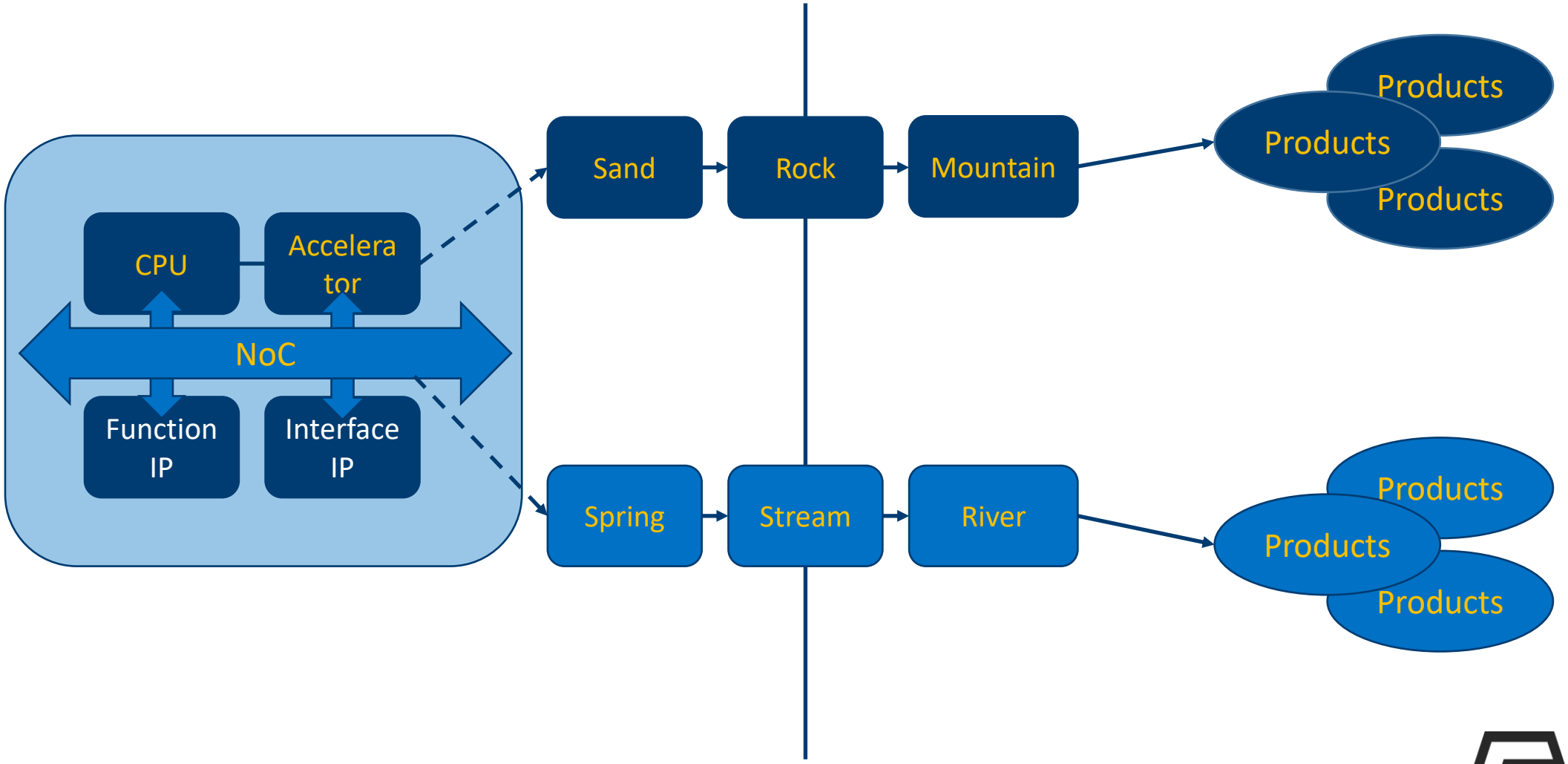
本文档是 *Chisel* (Constructing Hardware In a Scala Embedded Language) 的介绍性教程。Chisel 是一种嵌入在高阶编程语言 Scala 中用来构造硬件的语言。在未来的某个时候我们将提供更适合的参考手册，引入更多的教程示例。在这之前，本文档虽然有一些尝试和错误，但也应该可以带你开始使用 Chisel。Chisel

综合，实际上很多语法概念完全不是可综合的。另一些语法概念在如何映射到硬件实现方面是非常不直观的，或者一不小心就会导致非常低效的电路结构。使用这些语言的一个子集生成合意的结果未尝不可，然而它们表达的规范模型毕竟是杂乱和混淆的，在教学过程中这些现象尤其明显。

而且，我们开发新的硬件语言的强烈冲动来自于我们对改变现有的电子系统的设计方法的

SiFive

Sifive China Focus: Sand River



SiFive

Chisel Capabilities

- Chisel for library developers
  - Chisel provides hardware components (Reg, Wire, Mem, Mux, IO, etc…)
  - Chisel provides constructs (Vec, Bundle, Module, “:=“, “<>”, functionals
- Chisel for circuit designers
  - Diplomacy for two phase parameter negotiation and construction
  - Traits for easy RocketSystem expansion
- Chisel for product users
  - Easy configuration system for DSA exploration
  - Web-based GUI for end-user selection and integration

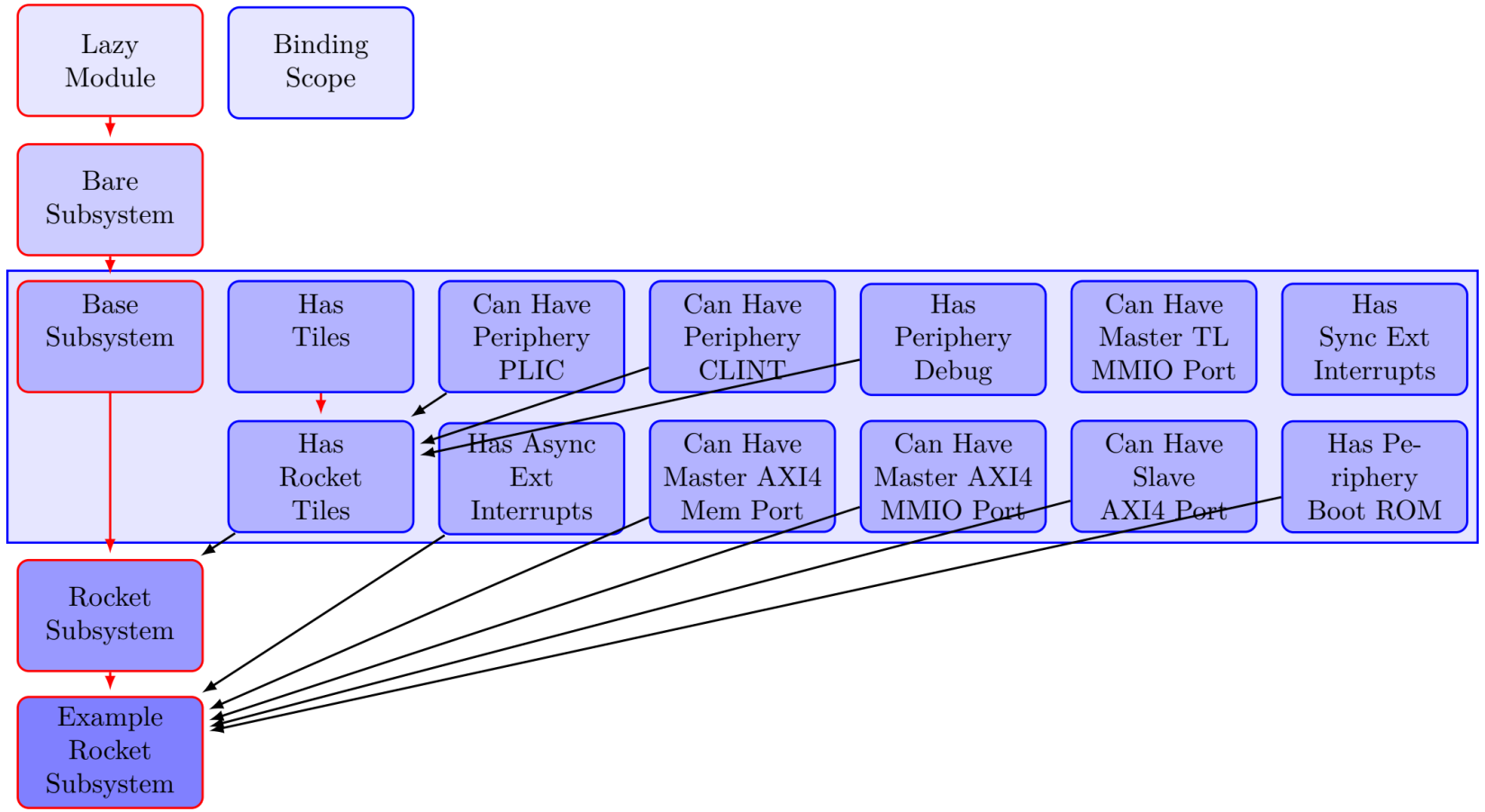
SiFive

An Rocket-Chip System Example

Library developer

Circuit developer

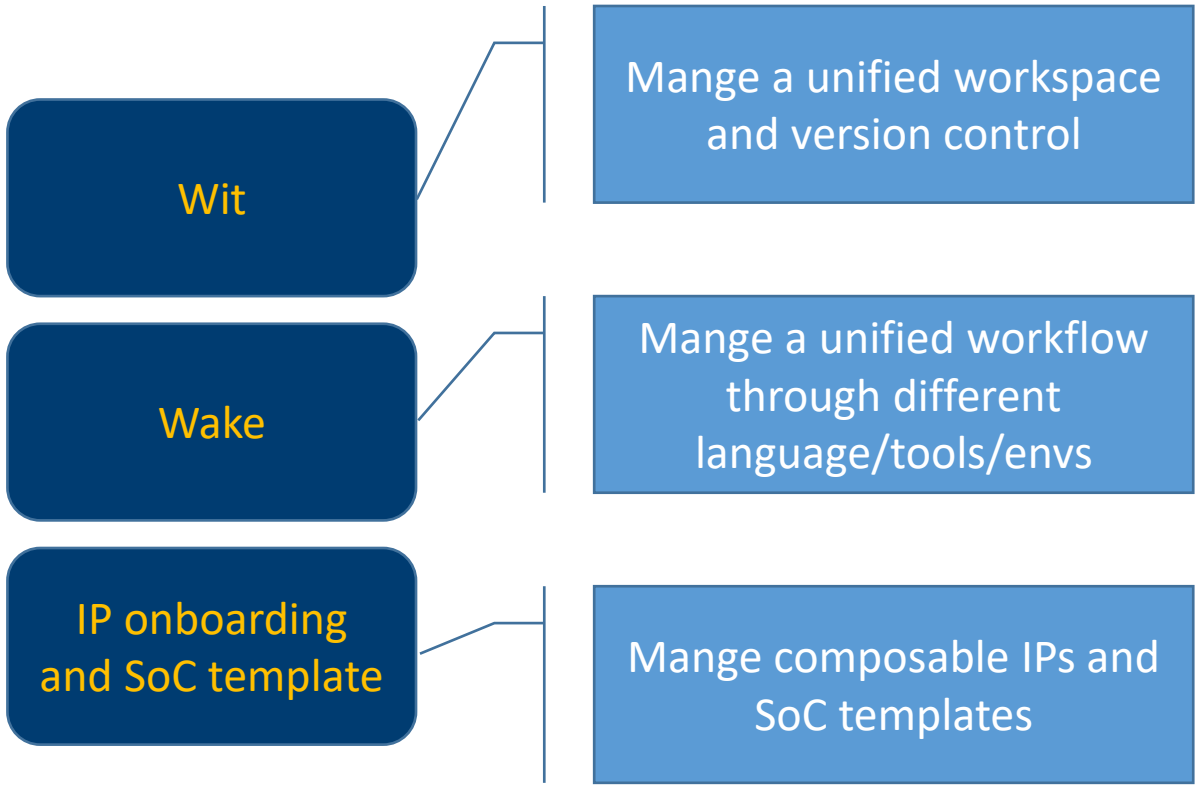
Product developer



SiFive

Technology Democracy Driven by Sifive

- Each chip player has its own IT/EDA flow
- Sifive drives an open flow for everyone
  - Enables small talented team
  - Boosts productivity by open, executable and exchangeable standards
  - Creates a highly convergent community

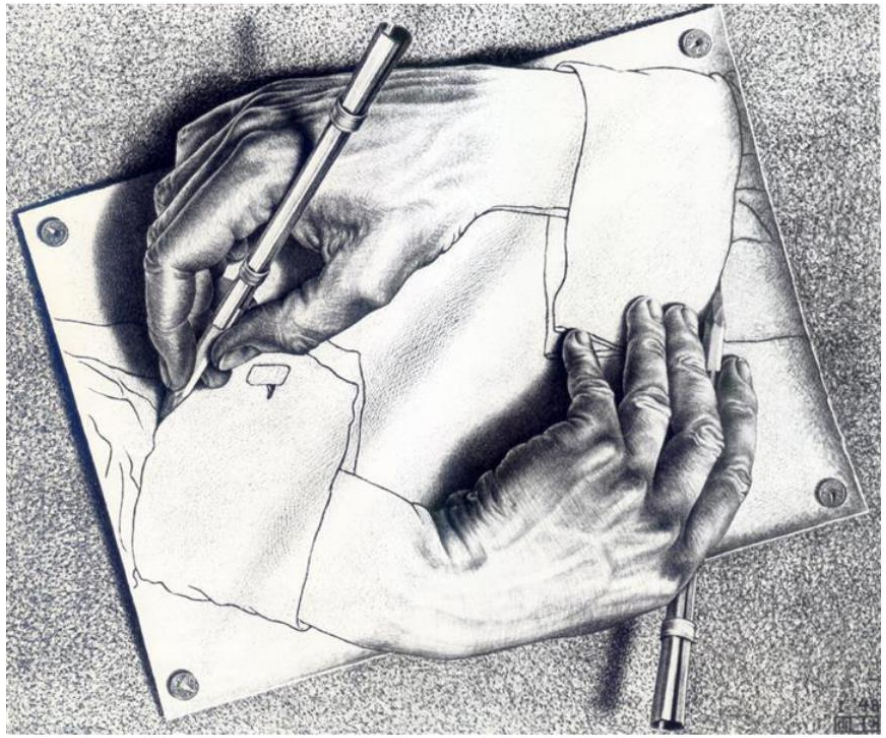


SiFive

One Trend of Chip Industry

Chisel: the Tool For AI Self-Design

Liwei Ma
Sifive China



SiFive

Talk at Sifive Tech Workshop, March, 2019, Liwei Ma

SiFive

Chip Industry Refactoring

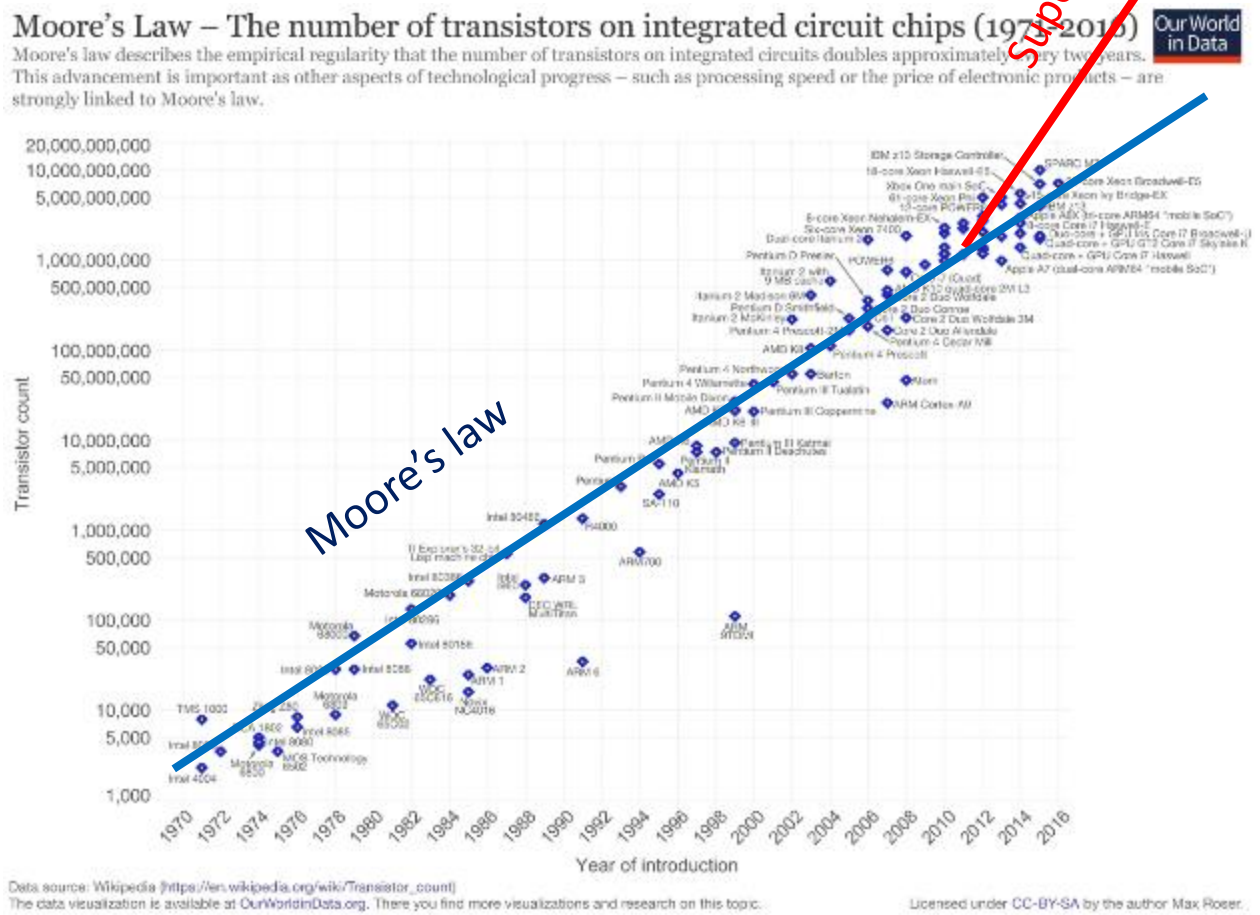
- Open and interoperable IP
  - Small talented teams win
- AI-based SoC PPA exploration
  - Design automation to intelligence
- Serve industry 4.0 in an industry 4.0 way
  - Internal industrial process externalization

SiFive

谢谢！

The Begin of Super Moore's Law

- Moore's law focuses on the doubled content
  - Frequency, transistor #, memory size, etc.
- Super Moore's law focuses on the doubling cadence
  - Every 9-12 months for one generation
  - Deep integration of industrial chain and ecosystem



SiFive