SiFive RISC-V Core IP

Product Map

	2 Series **Power & area optimized** 2–3-stage single-issue pipeline	3/5 Series **Efficient performance** 5–6-stage single-issue pipeline	7 Series **High performance** 8-stage, dual-issue superscalar pipeline	8 Series **Maximum performance** 3-wide 12-stage out-of-order superscalar pipeline
E Cores **32-bit embedded** MCU, edge computing, AI, IoT	**E2 Series** Our smallest, most efficient cores > **E24, E21, E20 Standard Cores** Compare to Cortex-M0+, M4, M4F	**E3 Series** Balanced performance and efficiency > **E34, E31 Standard Cores** Compare to Cortex-R5, R5F	**E7 Series** High performance 32-bit embedded cores > **E76, E76-MC Standard Cores** Compare to Cortex-M7	
S Cores **64-bit embedded** 8-stage, dual-issue pipeline	**S2 Series** Area-optimized 64-bit microcontrollers > **S21 Standard Core** No Arm equivalent	**S5 Series** Low-power 64-bit microcontrollers > **S51, S54 Standard Cores** Compare to Cortex-R5, R5F	**S7 Series** High performance 64-bit embedded cores > **S76, S76-MC Standard Cores** Compare to Cortex-R8	
U Cores **64-bit application cores** Linux, datacenter, network baseband		**U5 Series** Linux-capable application processors > **U54, U54-MC Standard Cores** Compare to Cortex-A53	**U7 Series** High performance Linux-capable processors > **U74, U74-MC Standard Cores** Compare Cortex-A55, A55 MP4	**U8 Series** Highest performance application processors > **U84, U87 Standard Cores** Compare to Cortex-A72

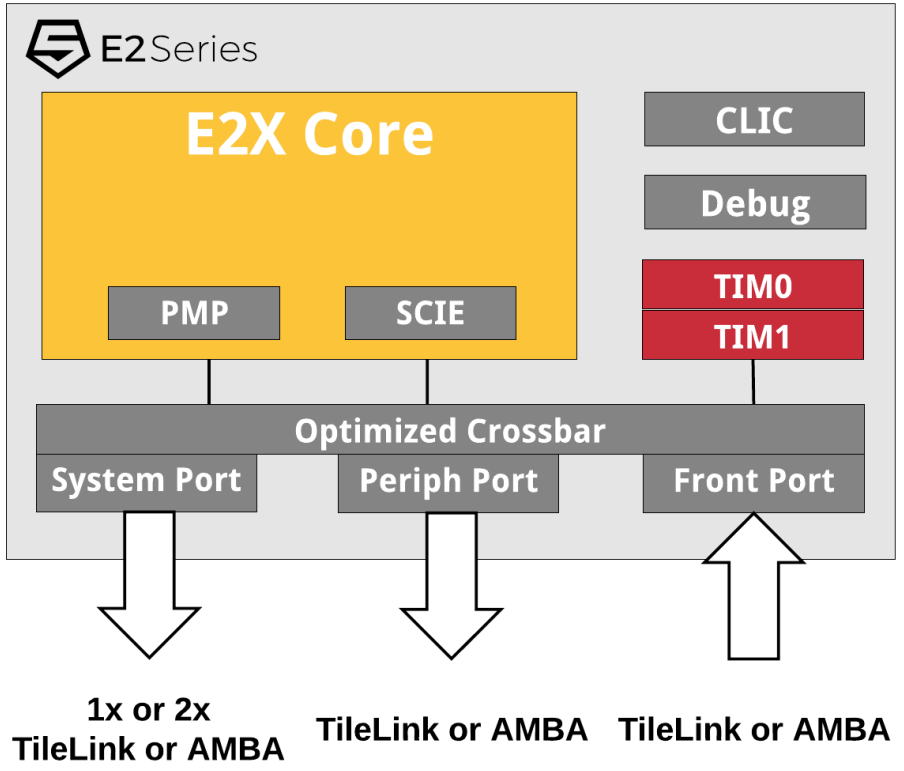
SiFive Core IP 2 series:

SiFive's **smallest** and most **efficient** RISC-V processor IP

E2 Series Features

The Smallest, Most Efficient RISC-V MCU Family

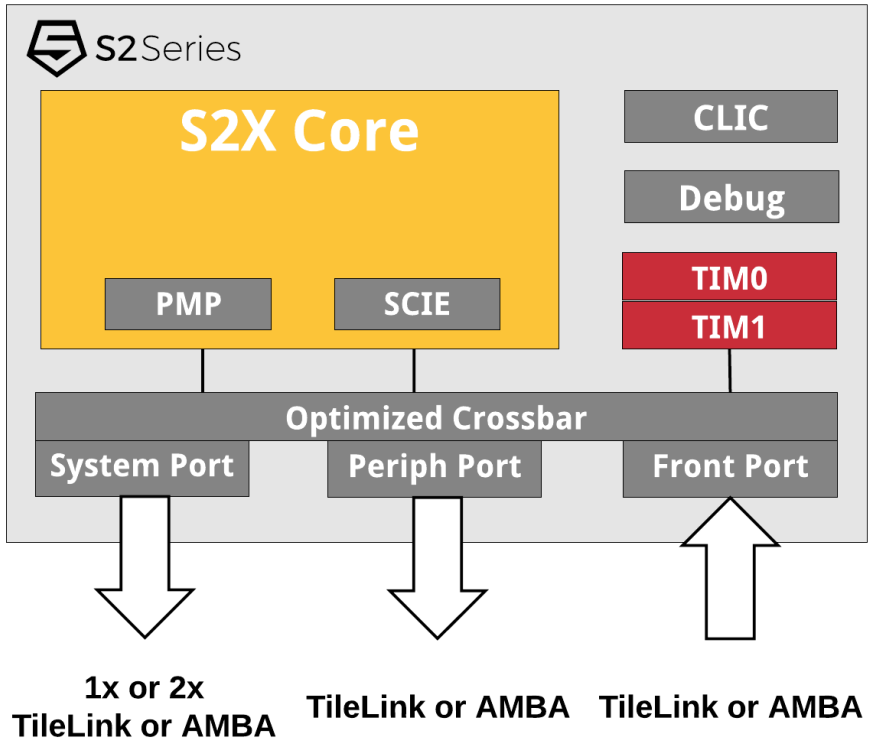
- **E2 Series core architectural overview**
  - RV32(E)IMAFDCV capable core
  - 2-3 stage, optional, Harvard Pipeline
- **Efficient memory accesses**
  - Ability to add multiple outbound Ports
  - Optional Tightly Integrated Memory (TIM) and Optional Instruction Cache
- **First RISC-V core with support for the RISC-V Core Local Interrupt Controller (CLIC)**
  - Provides hardware interrupt prioritization and nesting
  - Only 6 cycles to execute the first instruction of IRQ
- **SiFive Custom Instruction Extension (SCIE)**
  - Easily add support for custom instructions



S2 Series Features

The Smallest 64-bit MCU

- **S2 Series core architectural overview**
  - RV64IMAFDCV capable core
  - 2-3 stage, optional, Harvard Pipeline
- **Same familiar pipeline and feature set as the the E2 series but with 64-bit performance**
  - Increased DMIPs/MHz to 1.6 DMIPs/MHz
  - 64-bit arithmetic operations
  - Double the Load/Store bandwidth
- **Easier integration into larger SoCs**
  - S2 Series can directly address >32-bit physical address space
- **No impact on code size thanks to RISC-V Compressed instruction set**
  - The RISC-V RV64IC ISA uses the same 16-bit and 32-bit instructions as the RV32IC ISA



50% Smaller Core Area than a similarly spec'd S5

Area Constrained

Use **SiFive Core Designer** to configure the E2 Series Core to be as small as 13.5k Gates

Balanced

The E20 Standard Core is 90% the performance of Cortex-M3 in 60% of the area

High Performance

The E21 Standard Core which is 12% higher performance than Cortex-M4 in 80% of the area

64-bit MCU

S2 Series is the world's smallest 64-bit CPU offering ease of integration and efficient performance

2 Series - Impact of Configuration Options on Area

Choose between ISA

- **RV32EC - 16 integer registers**
  - less area, slight performance impact
- **RV32IC - 32 integer registers**
  - larger area, higher performance

Choose the interrupt controller

- **CLINT - Simple controller**
  - Up to 16 direct interrupts, in addition to architectural Timer and Software interrupts, with static priorities
  - Requires external controller for additional interrupts
- **CLIC - Featureful controller**
  - Up to 1008 interrupts
  - Dynamic prioritization with hardware vectoring and nesting
  - Can also connect an external controller for platform level interrupt sharing

Choose Performance Options

- 1 or 2 core interfaces - Von Neumann vs Harvard Architecture
- Multiplication Performance
- Hardware Floating Point Unit

Option	Gates (k)	Notes
RV32EC	13.5	Base Configuration
RV32IC	18.6	Base Configuration
CLINT	2.5	Basic irq controller with 16 irq
CLIC w/32 IRQ and 2 priority bits	6.0	E20 config
CLIC w/127 IRQ and 4 priority bits	16.3	E21 config
Seperate Data Interface	13.2	Harvard Architecture, E21 config
1 Cycle Mul	3.9	Includes 1 bit/cycle with early out DIV
4 Cycle Mul	1.7	Includes 1 bit/cycle with early out DIV
8 Cycle Mul	1.2	Includes 1 bit/cycle with early out DIV
FPU	31.7	
TL2AHB	2.4	per bridge
Debug	7.0	
all data from trails at 28HPC at 50MHz		
Gate Used (um2): ND2D0BWP35P140LVT		0.378

All of this and more configured directly from the web via SiFive Core Designer

E2 Series VS ARM Cortex-M

The E2 Series can be configured to meet your application requirements

E2 Series VS ARM Cortex-M Comparison Table						
	E2 Series Options	E20 Standard Core	E21 Standard Core	Cortex-M0+	Cortex-M3	Cortex-M4
Dhrystone (using GCC)	From 1.07 to 1.47 DMIPS/MHz	1.2 DMIPS/MHz	1.47 DMIPS/MHz	0.95 DMIPS/MHz	1.25 DMIPS/MHz	1.25DMIPS/MHz
CoreMark (using GCC)	Up to 3.1	2.5 CoreMarks/MHz	3.1 CoreMarks/MHz	1.8 CoreMarks/MHz	2.76 Coremarks/MHz	2.76 CoreMarks/MHz
Integer Registers	31 Useable, 16 Useable Option	31 Useable	31 Useable	13 Useable	13 Useable	13 Useable
FPU	Optional FPU	None	None	None	None	Optional
Hardware Multiply and Divide	Yes, Optional	Yes	Yes	Hardware Multiply Only	Yes	Yes
Memory Map	Customizable	SiFive Freedom Platform	SiFive Freedom Platform	Fixed ARMv6-M	Fixed ARMv7-M	Fixed ARMv7-M
Atomics	Optional: RISC-V standard AMO support via Peripheral Port and TIMs	No Peripheral Port	RISC-V AMO standard support via Peripheral Port	None	Bit-band and Load/Store Exclusive	Bit-band and Load/Store Exclusive
Number of Interrupts	Up to 1008 peripheral interrupts	32	127	32	240	240
Interrupt Latency into C Handler	6 Cycles – CLIC Vectored Mode	6 Cycles	6 Cycles	15 Cycles	12 Cycles	12 Cycles
Memory Protection	Optional up to 16 Regions	N/A	4 Regions	Optional, ARMv6m	0 or 8 Region	0 or 8 Region
Tightly Integrated Memory	Optional 2 Banks	None	2 Banks	No	No	No
Bus Interfaces	Configurable: Up to 3 masters and 1 slave with support for TileLink, AXI, AHB-Lite, APB	1 Master	2 Master, 1 Slave	1 AHB-Lite	3 AHB-Lite	3 AHB-Lite

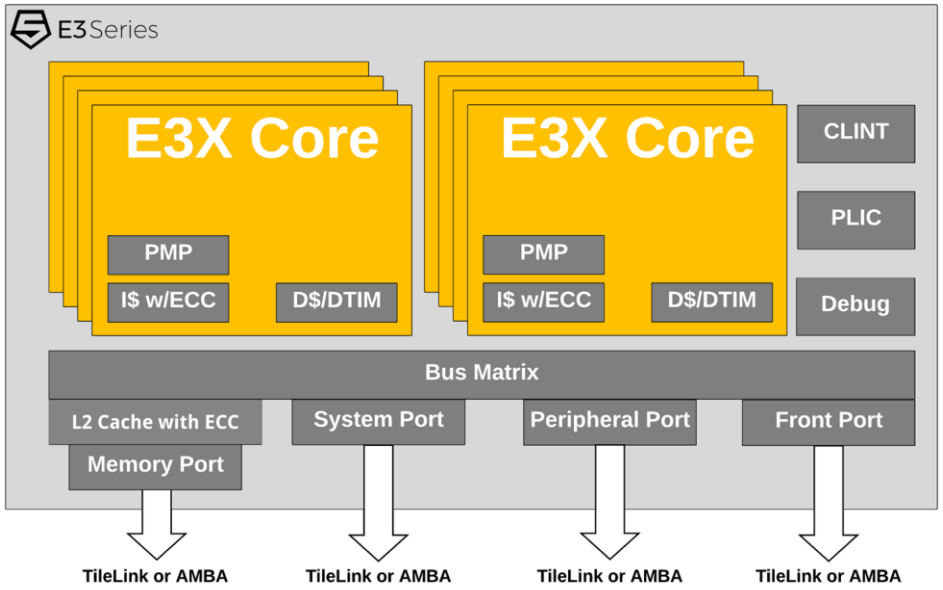
SiFive Core IP 3 and 5 series:

The **world's most deployed** RISC-V processor IP

E3/S5 Overview

High Performance, efficient, 32bit and 64bit RISC-V MCUs

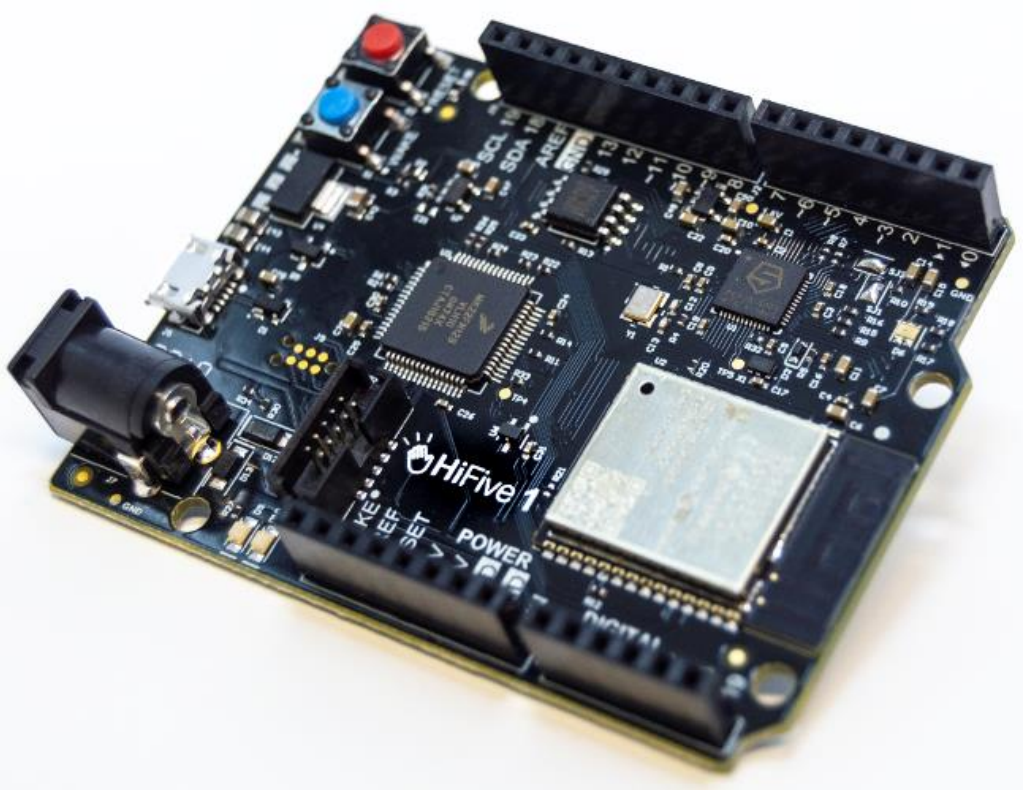
- **Flexible memory architecture**
  - I-Cache can be reconfigured into I-Cache + ITIM
  - DTIM for fast on Core Complex Data Access (D-Cache option also available)
  - Off Core Complex memory access through Memory, System and Peripheral Ports
- **Multicore Support**
  - Pre-integrated and verified by SiFive
  - Supports up to 8+ cores
- **Fast Interrupts**
  - E3/S5 with Interrupt Handlers in ITIM can enter an ISR in **10** cycles
  - CLIC Interrupt Controller for hardware interrupt prioritization and nesting
- **Security and Safety**
  - Up to 16 region physical memory protection
  - Optional ECC/Parity for all Level 1 and Level 2 memories
- **Real Time Capabilities**
  - Software enable/disable of dynamic branch prediction
  - Deterministic capabilities in the L1 and L2 Memories



	E31 (AHB)*	S51 (AXI)**	Cortex-R5***
28nm Area	0.066m2	0.126mm2	0.21mm2
Max Frequency	1.5GHz Typical	1.5GHz Typical	1.4GHz
Efficiency	155 DMIPS/mW	109 DMIPS/mW	62 DMIPS/mW

*E31 w/ AHB Ports, PLIC w/ 127 IRQ, Debug w/ 4 hw breakpoints, CLINT, area does not include RAMs
**E51 w/ AXI Ports, PLIC w/ 255 IRQ, Debug w/ 4 hw breakpoints, CLINT, area does not include RAMs
***unknown configuration: https://developer.arm.com/products/processors/cortex-r/cortex-r5

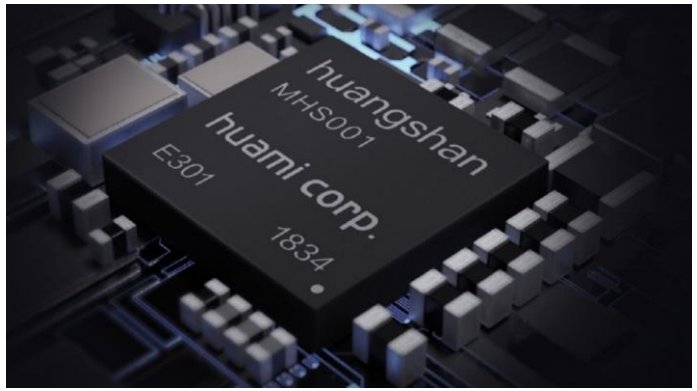
HiFive1 Rev B: Embedded RISC-V Dev Board



- SiFive FE310-G002 (built in 180nm)
  - Uses the E31 Standard Core
- Operating Voltage: 3.3 V and 1.8 V
- Input Voltage: 5 V USB or 7-12 VDC Jack
- IO Voltages: 3.3 V only
- Digital I/O Pins: 19
- PWM Pins: 9
- SPI Controllers/HW CS Pins: 1/3
- Hardware I2C: 1
- UART: 2
- External Interrupt Pins: 19
- External Wakeup Pins: 1
- Flash Memory: 4 MB Quad SPI
- Host Interface (microUSB): Program, Debug, and Serial Communication

Order on Crowdsupply

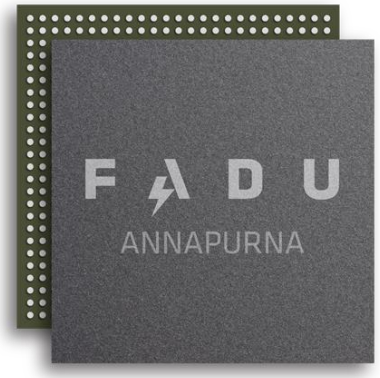
E3 Series



"SiFive's RISC-V Core IP was **1/3 the power** and **1/3 the area** of competing solutions, and gave FADU the flexibility we needed in optimizing our architecture to achieve these groundbreaking products."

-J. Lee, FADU CEO

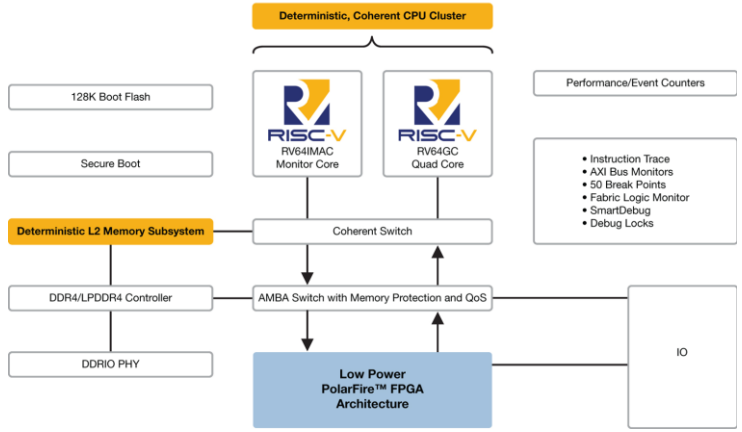
S5 Series



"SiFive's **64-bit S Cores** bring their hallmark efficiency, configurability and **silicon-proven** Core IP **expertise** to 64-bit embedded architectures"

-Ted Speers, Head of Product Architecture and Planning, Microsemi, a Microchip Company

U5 Series



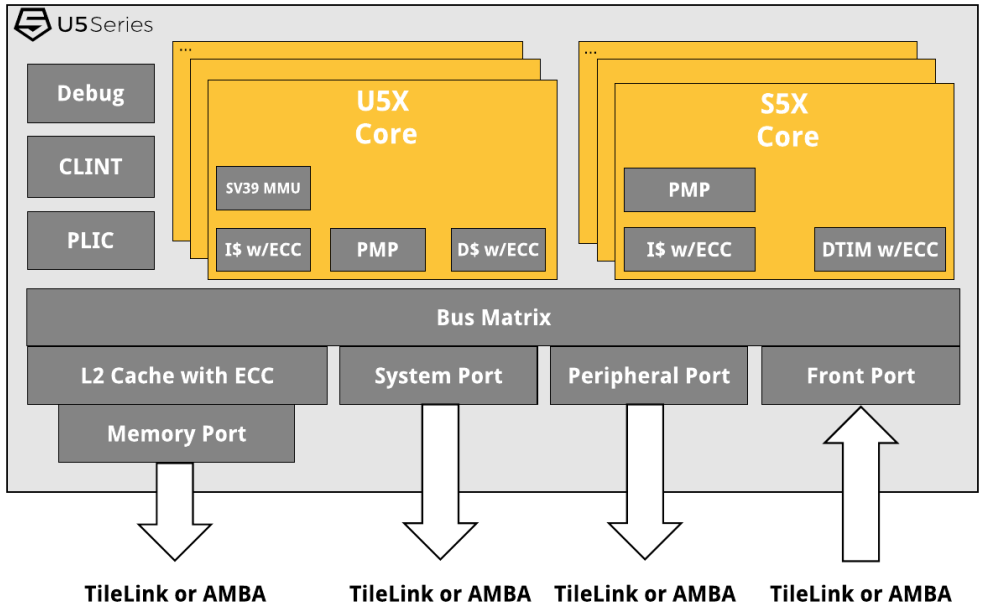
"SiFive's RISC-V Core IP was **1/3 the power** and **1/3 the area** of competing solutions, and gave FADU the flexibility we needed in optimizing our architecture to achieve these groundbreaking products."

-J. Lee, FADU CEO

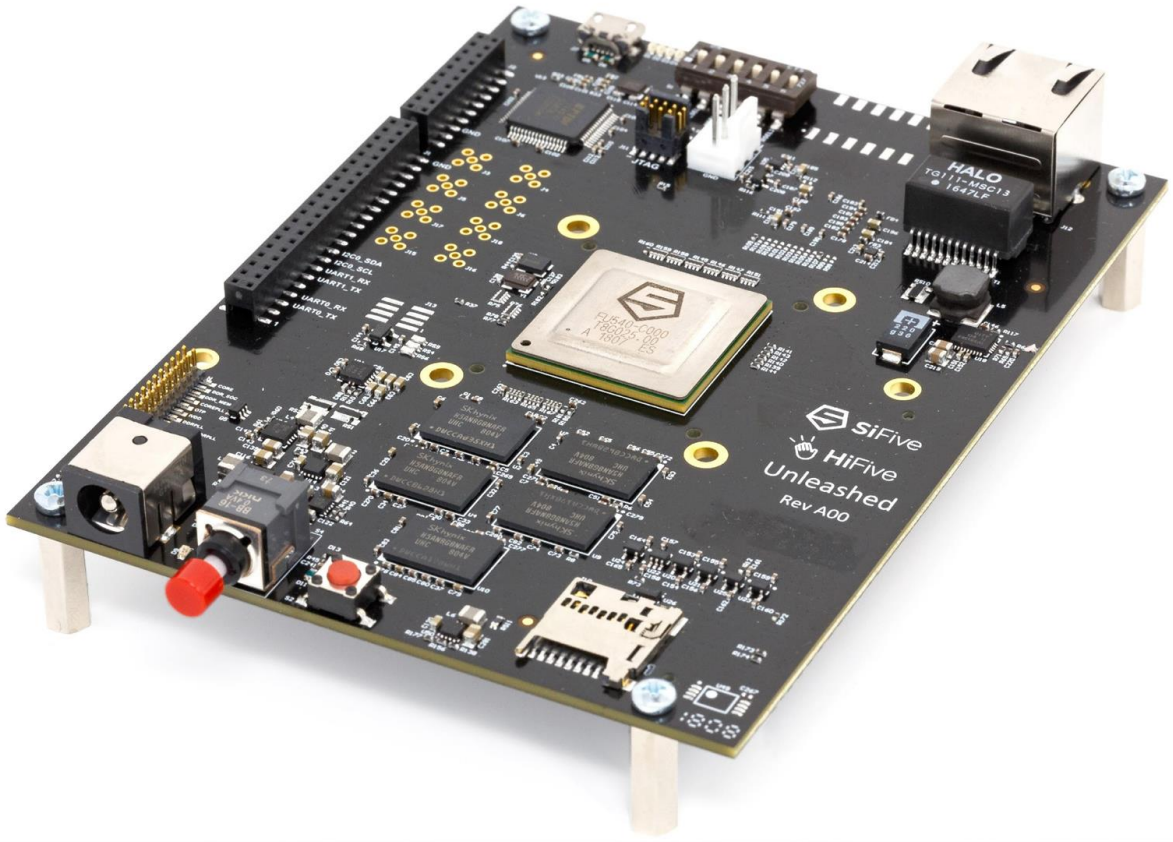
U5 Series Features

64-bit RISC-V Multi-Core Linux-Capable

- **U5 Series allows for instantiation of up to 9 U5 and/or S5 cores as well as a configurable Level 2 Cache**
- **U5 Core Architectural Features**
  - RV64GCN capable core with Sv39 Virtual Memory Support
  - Single Issue, in-order 5-6 stage Harvard Pipeline
  - Optional SECDED ECC support on Level 1 and Level 2 memories
- **Flexible memory system allows for application specific resource partitioning**
  - L2 can be split into part cache, part fast addressable RAM
- **Configurable, coherent, S5X minion cores can provide a variety uses**
  - System boot and monitor, Sensor Hub/Fusion, Security Co-Processor
- **Real Time Capabilities**
  - Software enable/disable of dynamic branch prediction
  - Deterministic L1 and L2 Memories
- **Broad market applications**
  - General purpose embedded, industrial, IoT, high-performance real-time embedded, automotive



HiFive Unleashed: World's First Multi-Core RISC-V Linux Dev Board

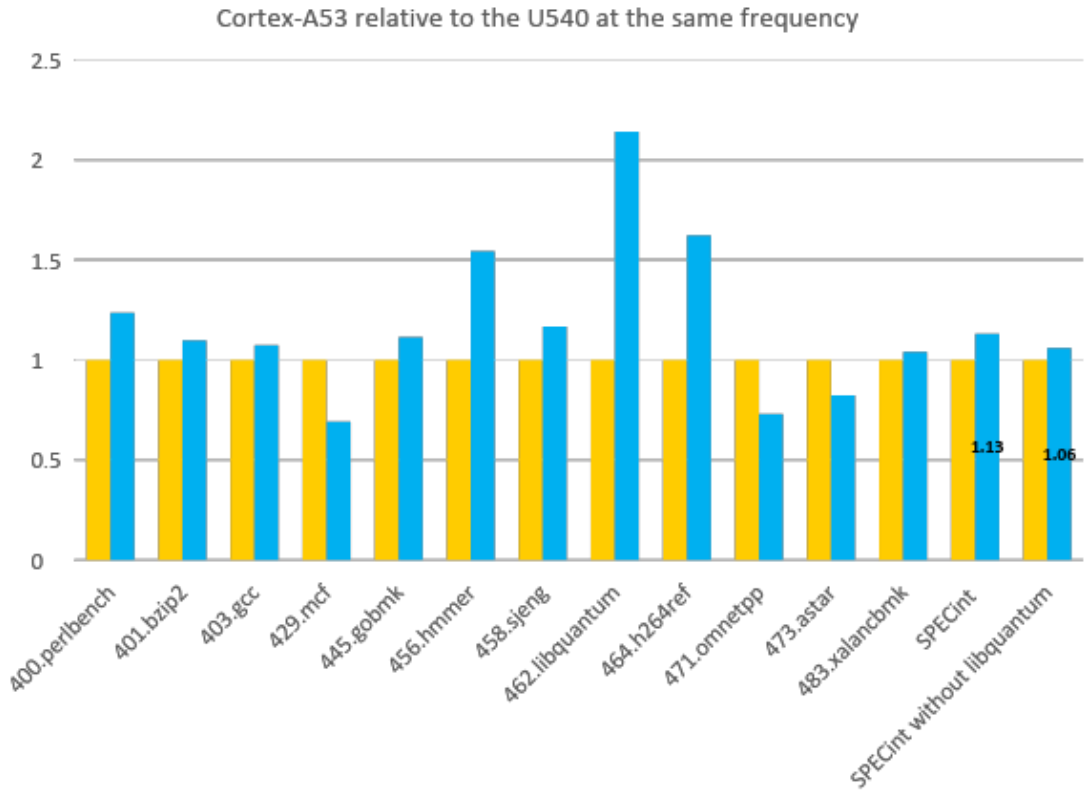


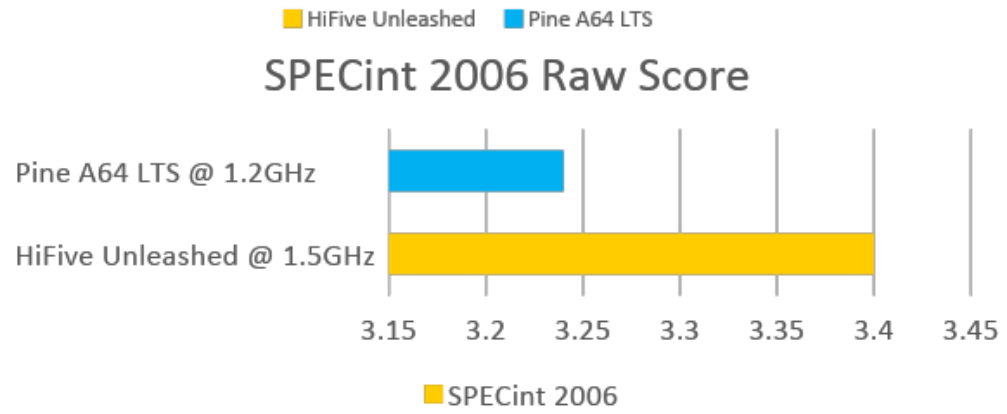
- SiFive FU540-C000 (built in 28nm)
  - Uses the U54-MC Standard Core
- 8 GB 64-bit DDR4 with ECC
- Gigabit Ethernet Port
- 32 MB Quad SPI Flash
- MicroSD card for removable storage
- MicroUSB for debug and serial communication
- Digital GPIO pins
- FMC connector for future expansion with add-in cards

Order now at crowdsupply.com for $999

U54 Performance - Comparable to Cortex-A53

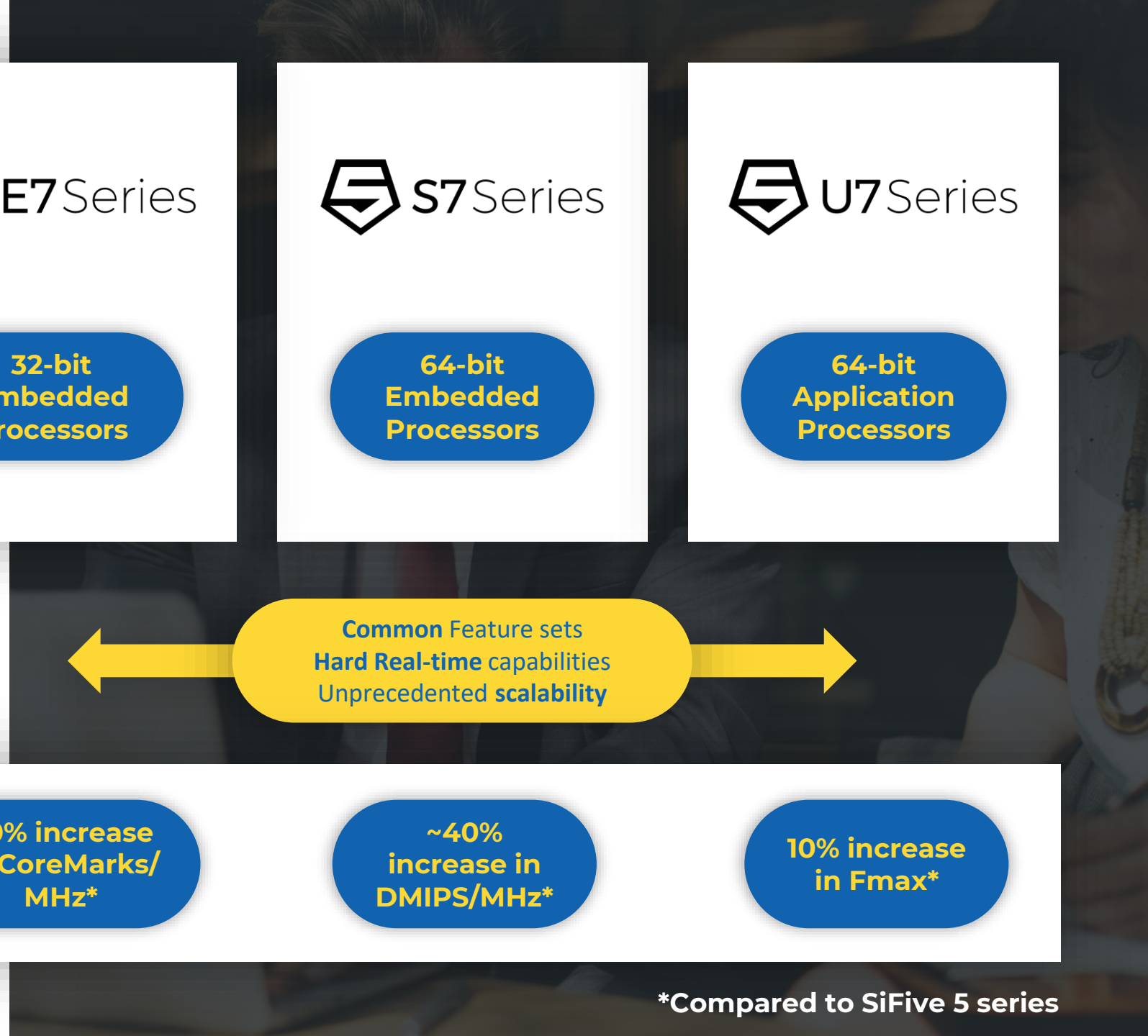
- **U54 SPECint 2006 - 3.40**
  - Measured at 1.5GHz on the U540-C000 Silicon on the HiFive Unleashed
- **HiFive Unleashed – SiFive FU540-C000 SoC**
  - 4x SiFive U54 1.5GHz
  - GCC 8 pre-release
- **Pine A64 LTS – Allwinner R18 SoC**
  - 4x Cortex-A53 1.2GHz
  - GCC 8 pre-release
- **The single-issue, in-order U54 core approaches the performance of a Cortex-A53 in *HALF* the area**





SiFive Core IP 7 series:

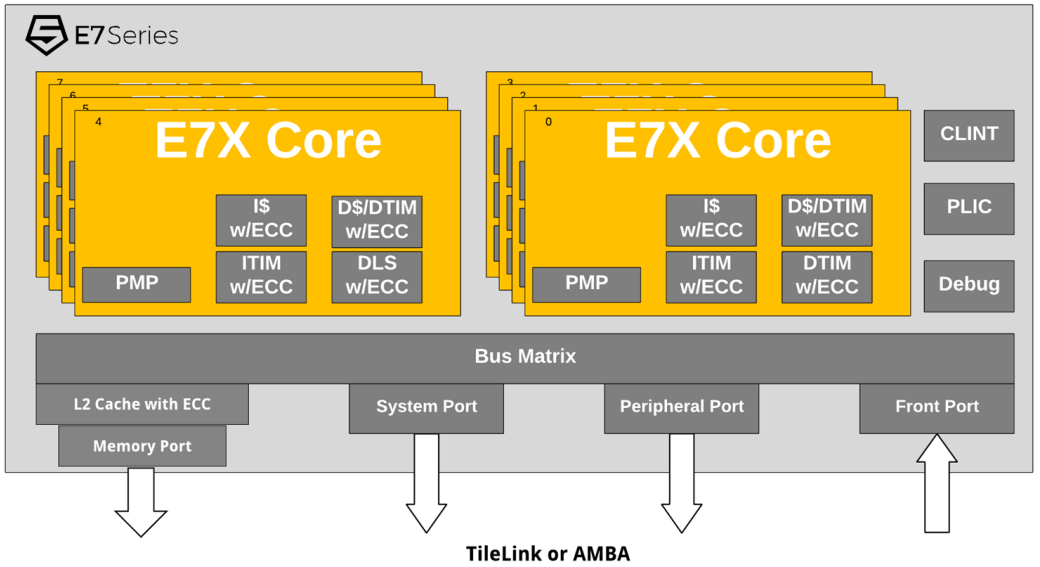
The **highest performance** commercial **RISC-V** processor IP



E7 and S7 Series Features

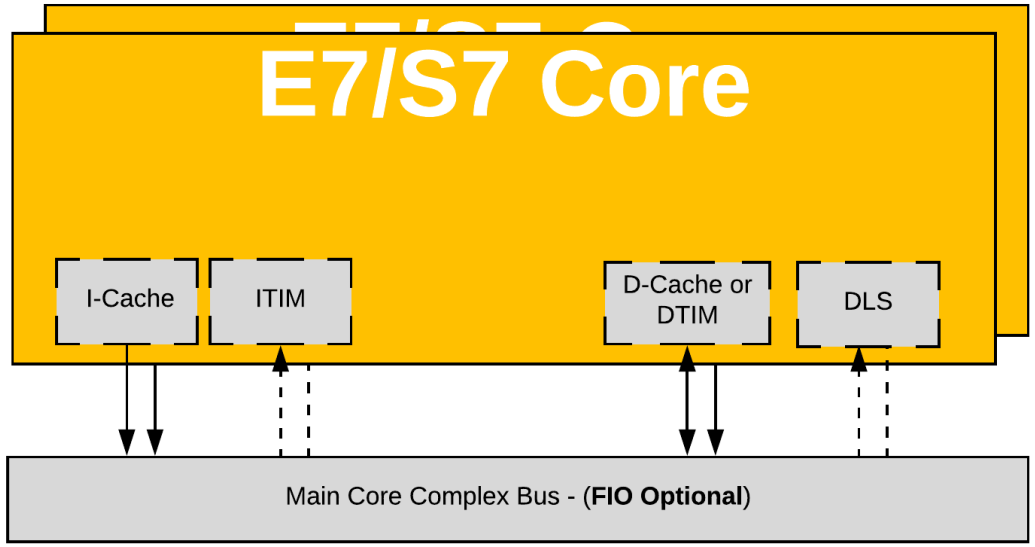
Ultra High Performance 64-bit RISC-V Embedded Processor

- **7 core architectural features**
  - RV32/64GCV capable core
  - Dual Issue, in-order 8 stage Harvard Pipeline
- **Performance and Area**
  - DMIPS – 2.5 DMIPS/MHz
  - Coremark – 5.1 CoreMarks/MHz
  - Core Area is only 30% larger than equivalent 3/5 Series Core
- **Very flexible memory system**
  - Optional I$ and D$
  - Optional I and D TCM interfaces
  - Optional Fast IO (FIO) for low latency, high-bandwidth, memory mapped IO
- **Functional Safety and Security and Real Time features**
  - SECDED ECC on all L1 and L2 memories
  - Programmatically clear and/or disable dynamic branch prediction for deterministic execution and enhanced security
- **Multi-Core Capable with Coherency and optional L2**
- **High end embedded applications**
  - SSD Controllers
  - IoT Edge Computing
  - Wireless Radios
  - Automotive/Industrial



7 Series Memory Subsystem

- **ITIM/DTIM**
  - Single-cycle memories on the Instruction or Data bus
  - Can have ***both*** an ITIM and I$
  - Can have ***either*** a DTIM or D$
  - Both supports Atomic instructions
  - Other masters can access ITIM/DTIM with additional latency
- **Data Local Store**
  - 4-cycle Load-Use for data accesses with pipelined loads/stores
    - Instruction accesses incur additional latency
  - Available in addition to a D$
  - Runs at the same frequency as the Core
  - Supports Atomics
  - Other Masters can access DLS with additional latency
- **Fast IO Option - 2x Load-Store Bandwidth**
  - Fast IO improves throughput of MMIO transactions in Core Complex memory subsystem by enabling a number of uArchitectural MMIO optimizations in the 7 Series pipeline
  - Will have an impact on top end frequency



	I$	D$	ITIM	DTIM	DLS
Load-use delay (cycles)	n/a	0	0	0	4
Support for Atomic Operations	yes	yes	yes	yes	yes

E7/S7 vs R5/R8

Feature	E7	S7	Arm Cortex-R5	Arm Cortex-R8
Instruction set architecture	RV32IMAFC	RV64IMAFDC	Armv7-R	Armv7-R
DMIPS/MHz	2.3/3.73	2.5/4.27	1.67/2.45	2.50/3.77
Cores	Up to 8 Cores AMP/SMP	Up to 9 Cores AMP/SMP	2-core AMP	Up to 4 Cores AMP/SMP
Heterogeneous	No; cannot be combined with U7 series cores	Yes; can be combined with U7 series cores	No; cannot be combined with Cortex-A cores	No; cannot be combined with Cortex-A cores
Pipeline	8-stage, dual issue, in order	8-stage, dual issue, in order	8-stage dual issue, in order	11-stage, superscalar, out of order
TIM	up to 256KB ITIM up to 256KB DTIM up to 512KB DLS	up to 256KB ITIM up to 256KB DTIM up to 512KB DLS	up to 8MB ITCM up to 8MB DTCM	up to 8MB ITCM up to 8MB DTCM
Caches	I-Cache:up to 64KB D-Cache:up to 256KB	I-Cache:up to 64KB D-Cache:up to 256KB	I-Cache:4-64KB D-Cache:4-64KB	I-Cache:4-64KB D-Cache:4-64KB
L2 Cache Controller	Optional, Pre-integrated up to 4MB,32-way,4Banks	Optional Pre-integrated up to 4MB,32-way,4Banks	external	external
FPU	single or double FP	single or double FP	Double Precision FPU	Double Precision FPU
MPU	up to 16-Regions	up to 16-Regions	up to 16-Regions	up to 24-Regions
Bus Matrix	Pre-integrated, Configurable	Pre-integrated, configurable	No	No
ECC	on L1/L2	on L1/L2	on L1/AXI bus ports	on L1/AXI bus ports
Frequency	E76: Typical: 1.4GHz [a] E76: Worst: 850MHz [a]	S76: Typical: 1.3GHz [a] S76: Worst: 825MHz [a]	AFAP: 1.4GHz [b1] FEATURED: 935MHz [b2]	AFAP: 1.5GHz [b1]
Area	E76: 0.174/0.09 mm^2 [c]	S76: 0.231/0.154 mm^2 [c]	0.21 mm^2 [d]	0.33 mm^2 [d]

Note:

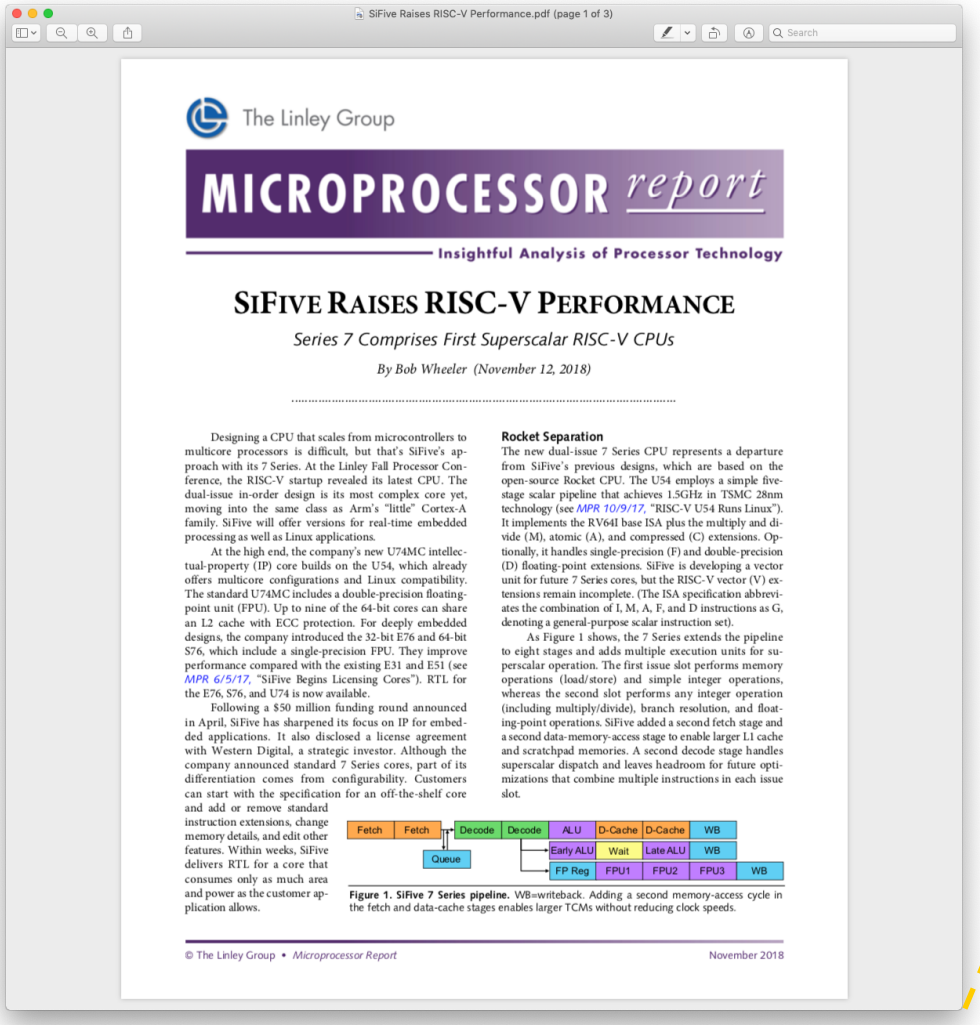
a. 28HPC,12 track standard cells. Typical: TT Corner @ 0.9V, 25C ,Worst: Slow/Slow, 0.81V, -40C

b. 28HPM, b1.sc12mc base svt (38.2%) /lvt (36.4%) c31, sc12mc hpk svt (5.8%) / lvt (9.6%) c31
b2.sc9mc base svt c31 (95.2%), sc9mc_cln28hpm_hpk_svt_c31 (4.8%)

c. Does not include RAMs, Core Complex/Core Only, see standard core configuration

d. Includes Core+RAM+Routing, smallest configuration

Linley MPR – “SiFive Raises RISC-V Performance”


SiFive Raises RISC-V Performance.pdf (page 1 of 3)

The Linley Group

MICROPROCESSOR report

Insightful Analysis of Processor Technology

SiFive Raises RISC-V Performance

Series 7 Comprises First Superscalar RISC-V CPUs

By Bob Wheeler (November 12, 2018)

Designing a CPU that scales from microcontrollers to multicore processors is difficult, but that's SiFive's approach with its 7 Series. At the Linley Fall Processor Conference, the RISC-V startup revealed its latest CPU. The dual-issue in-order design is its most complex core yet, moving into the same class as Arm's "little" Cortex-A family. SiFive will offer versions for real-time embedded processing as well as Linux applications.

At the high end, the company's new U74MC intellectual-property (IP) core builds on the U54, which already offers multicore configurations and Linux compatibility. The standard U74MC includes a double-precision floating-point unit (FPU). Up to nine of the 64-bit cores can share an L2 cache with ECC protection. For deeply embedded designs, the company introduced the 32-bit E76 and 64-bit S76, which include a single-precision FPU. They improve performance compared with the existing E31 and E51 (see *MPR 6/5/17*, "SiFive Begins Licensing Cores"). RTL for the E76, S76, and U74 is now available.

Following a $50 million funding round announced in April, SiFive has sharpened its focus on IP for embedded applications. It also disclosed a license agreement with Western Digital, a strategic investor. Although the company announced standard 7 Series cores, part of its differentiation comes from configurability. Customers can start with the specification for an off-the-shelf core and add or remove standard instruction extensions, change memory details, and edit other features. Within weeks, SiFive delivers RTL for a core that consumes only as much area and power as the customer application allows.

Rocket Separation

The new dual-issue 7 Series CPU represents a departure from SiFive's previous designs, which are based on the open-source Rocket CPU. The U54 employs a simple five-stage scalar pipeline that achieves 1.5GHz in TSMC 28nm technology (see *MPR 10/9/17*, "RISC-V U54 Runs Linux"). It implements the RV64I base ISA plus the multiply and divide (M), atomic (A), and compressed (C) extensions. Optionally, it handles single-precision (F) and double-precision (D) floating-point extensions. SiFive is developing a vector unit for future 7 Series cores, but the RISC-V vector (V) extensions remain incomplete. (The ISA specification abbreviates the combination of I, M, A, F, and D instructions as G, denoting a general-purpose scalar instruction set).

As Figure 1 shows, the 7 Series extends the pipeline to eight stages and adds multiple execution units for superscalar operation. The first issue slot performs memory operations (load/store) and simple integer operations, whereas the second slot performs any integer operation (including multiply/divide), branch resolution, and floating-point operations. SiFive added a second fetch stage and a second data-memory-access stage to enable larger L1 cache and scratchpad memories. A second decode stage handles superscalar dispatch and leaves headroom for future optimizations that combine multiple instructions in each issue slot.

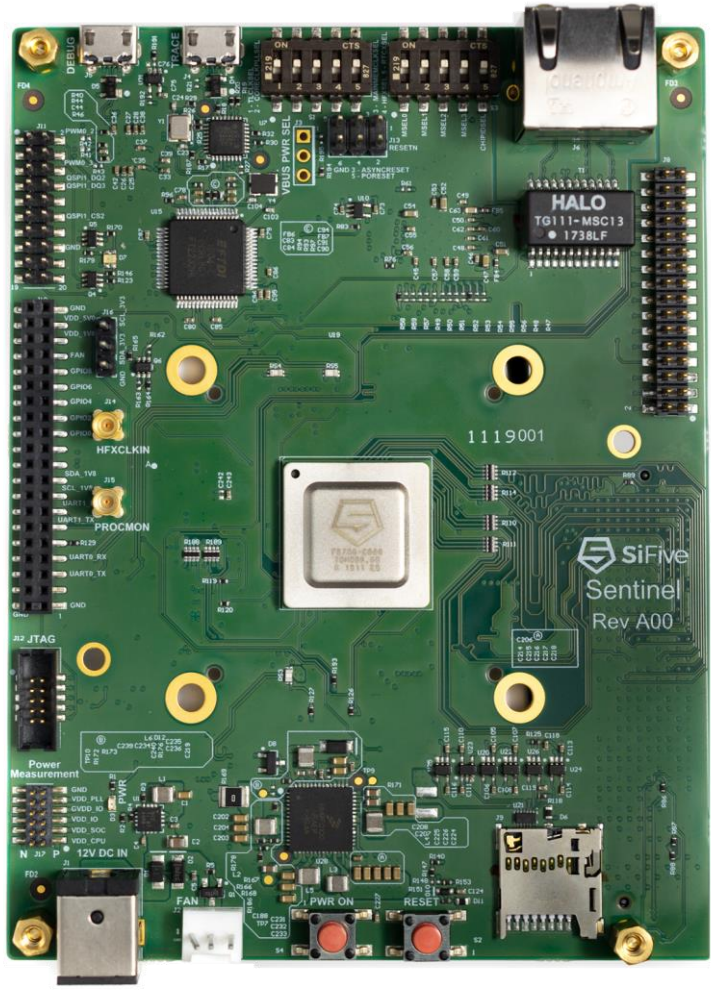
Figure 1. SiFive 7 Series pipeline. WB=writeback. Adding a second memory-access cycle in the fetch and data-cache stages enables larger TCMs without reducing clock speeds.

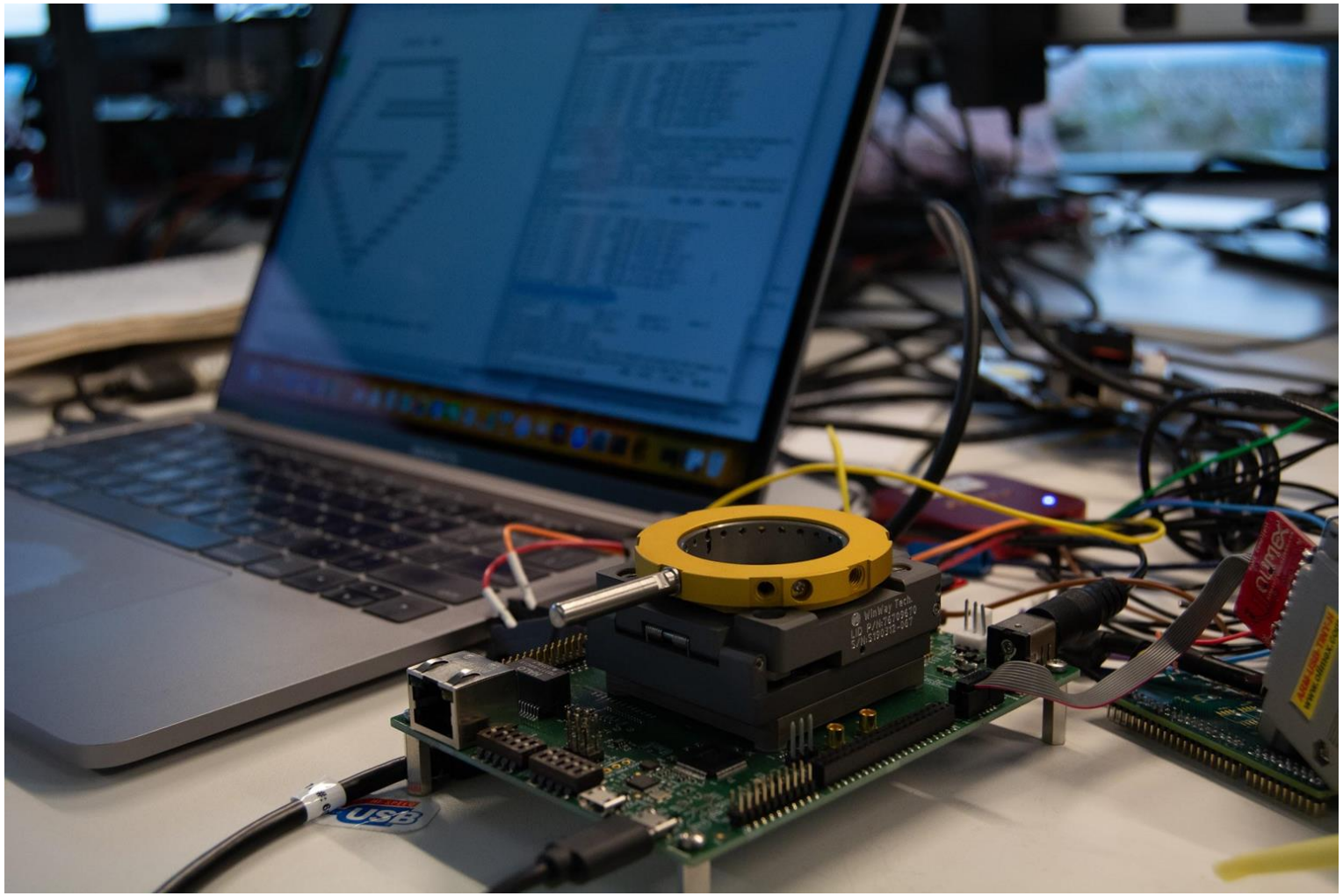
	SiFive E76	Arm Cortex-M7	SiFive U74	Arm Cortex-A55
Instruction Set	32-bit RISC-V	32-bit Arm v7-M	64-bit RISC-V	64-bit Arm v8
Max Clock Freq	1.6GHz†	1.1GHz	1.6GHz†	1.6GHz†
Max IPC	2 IPC	2 IPC	2 IPC	2 IPC
CoreMark Perf	4.9CM/MHz	5.0CM/MHz	4.9CM/MHz	4.4CM/MHz†
Die Area*	0.065mm²	0.067mm²	0.22mm²	0.65mm²†

Table 1. SiFive-versus-Arm CPU comparison. The new dual-issue 7 Series delivers integer performance on a par with that of Arm's comparable CPUs. All metrics assume TSMC 28nm HP technology. *Without memories. (Source: vendors, except †The Linley Group estimate)

source :
https://www.linleygroup.com/mpr/

SiFive 7 Series - Silicon Proven Core IP

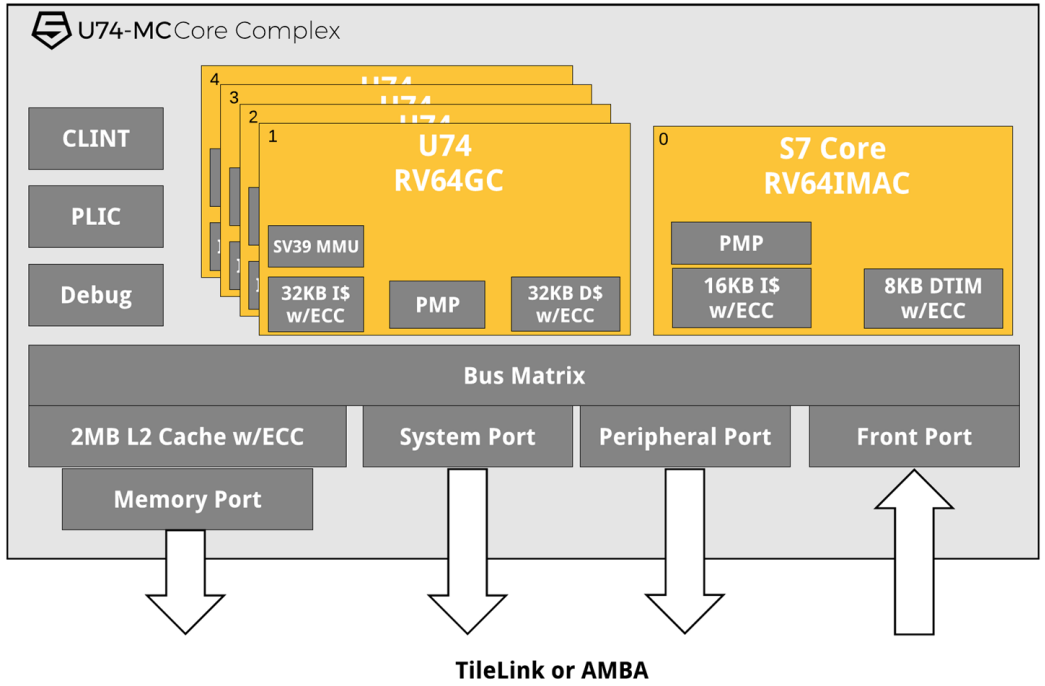




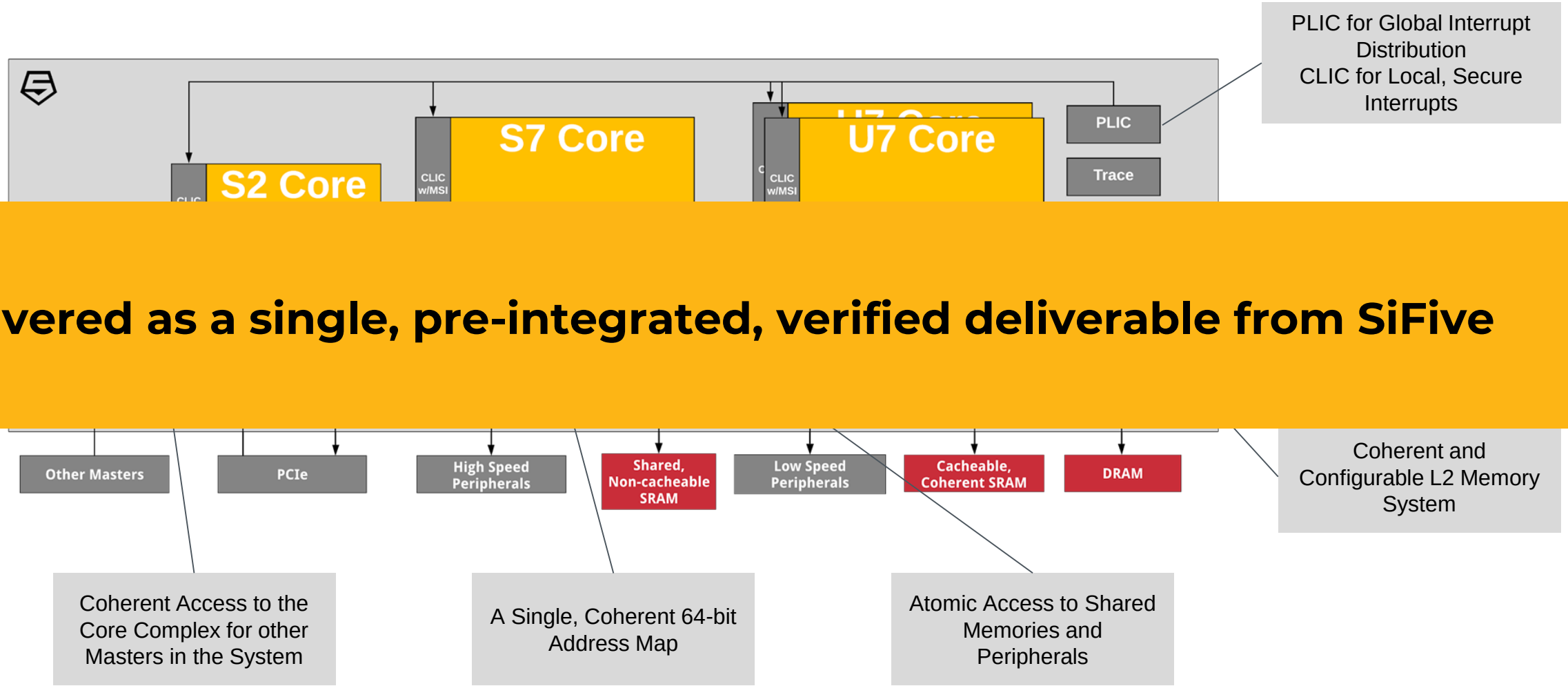
U7 Series Features

High Performance 64-bit RISC-V Multi-Core Application Processor

- **U7 allows for instantiation of up to 9 U7 and/or S5 cores as well as a configurable Level 2 Cache**
- **U7 Core Architectural Features**
  - RV64GCV capable core with Sv39 Virtual Memory Support
  - Dual Issue, in-order 8 stage Harvard Pipeline
  - Optional SECDED ECC support on Level 1 and Level 2 memories
- **Performance and Area**
  - 2.5 DMIPS/MHz
  - 5.1 Coremarks/MHz
  - SPEC2k6: U54 + 40%
- **Functional Safety and Security and Real Time features**
  - SECDED ECC on all L1 and L2 memories
  - Optional L1 and L2 Tightly Integrated Memories
  - Programmatically clear and/or disable dynamic branch prediction for deterministic execution and enhanced security
- **Configurable EXX minion cores can provide a variety uses**
  - System boot and monitor, Sensor Hub/Fusion, Security Co-Processor
- **Broad market applications**
  - General purpose embedded, industrial, IoT, high-performance real-time embedded, automotive



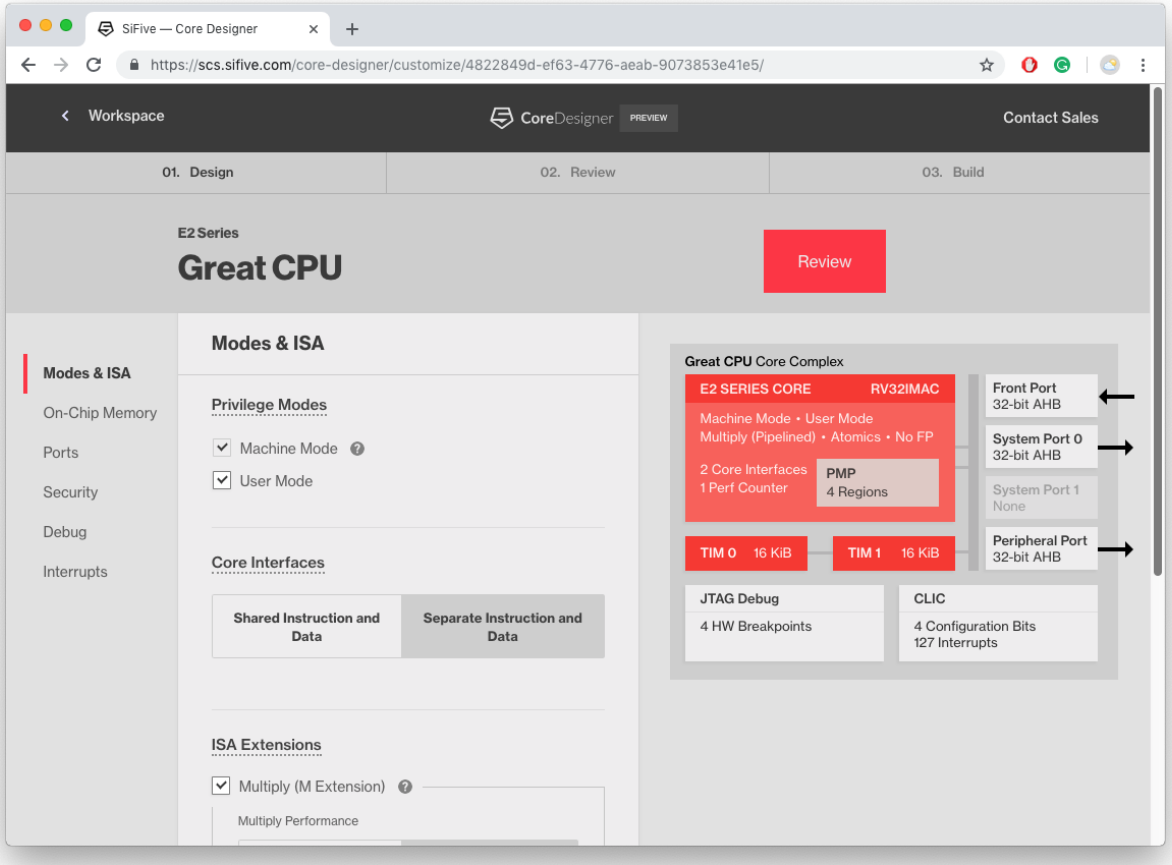
SiFive Mix and Match Combining Embedded and Application Cores



Delivered as a single, pre-integrated, verified deliverable from SiFive

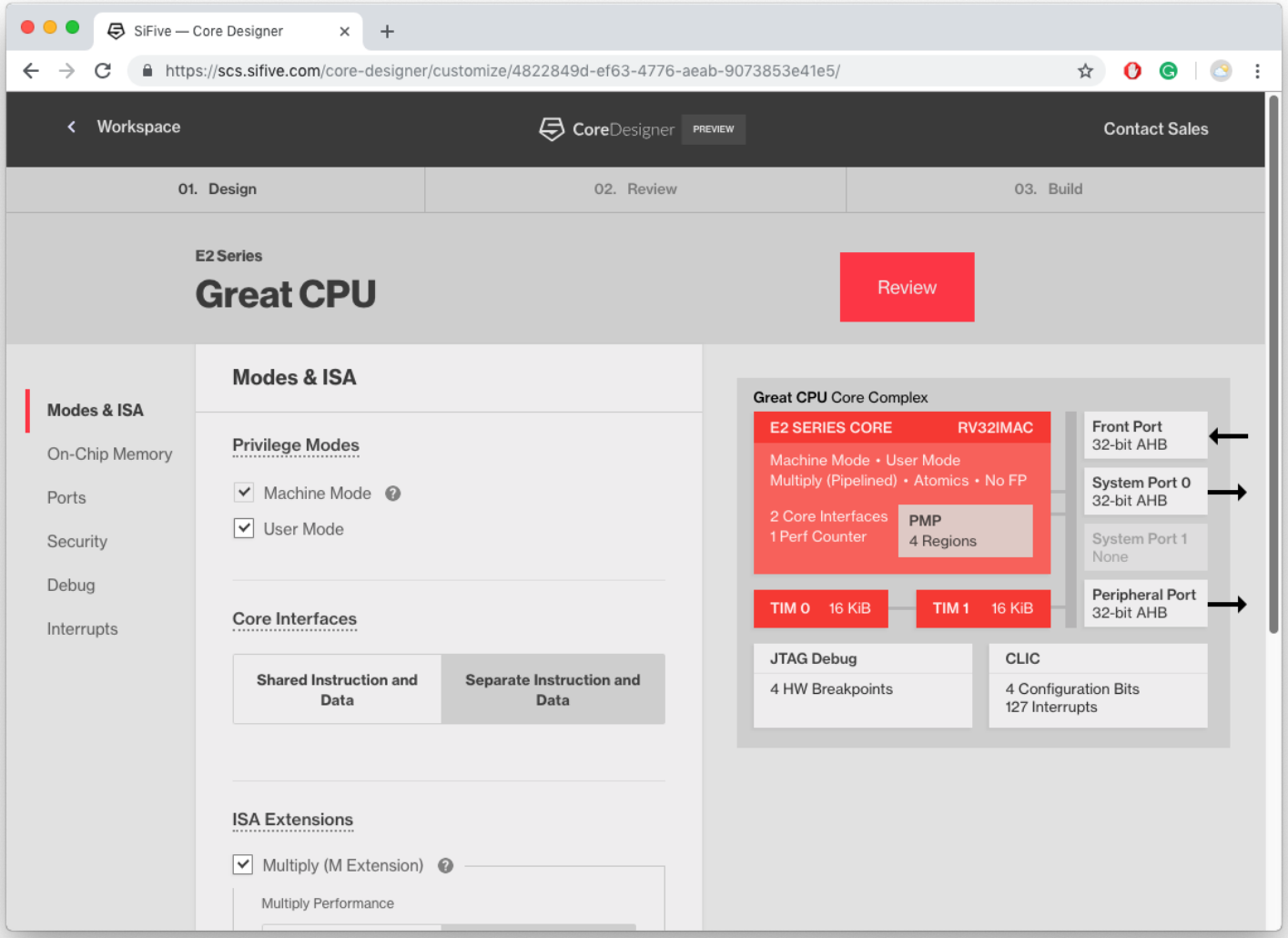
SiFive Core Designer

Your interface to SiFive RISC-V Core IP



- All SiFive Core IP is configured and delivered via the SiFive Core Designer Web Portal
  - Simple, Easy to Use, Web Interface
- **Variant** are generated with click of a button and available from the Workspace
- **Variants** contain
  - RTL matching the configuration, including a testbench, and other collateral needed to realize the design
  - Documentation specific to the design
  - Customized bare-metal BSP for easy integration into SiFive's SDKs
  - FPGA bitstreams for common FPGA development boards for easy software benchmarking of the RC

SiFive Core Designer Demo

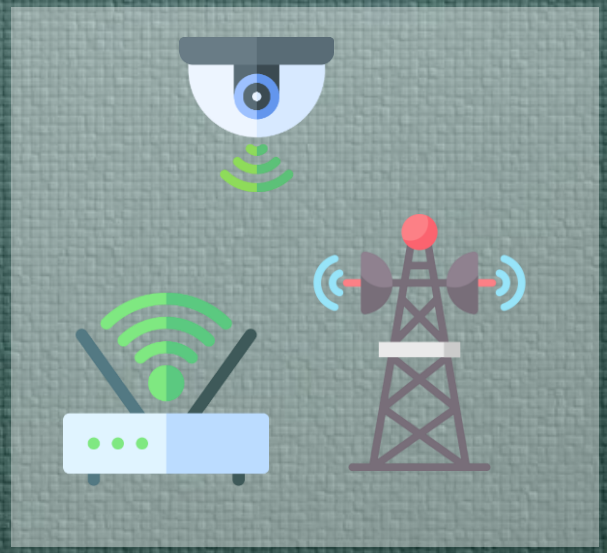


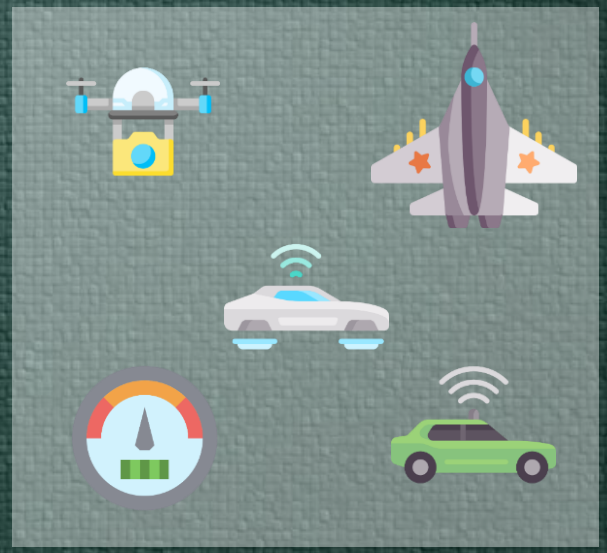
SiFive U8-Series

Incredibly Scalable **Out-of-Order** Application Processor Core IP

2017 2018 TODAY

Enabling Innovation For End Points, IoT Edge, and Cloud





End Points	Enterprise	Edge/Autonomous
DTV / Smart Home	5G Wireless	AV / ADAS
AR, VR, MR	Core/Edge Routers	IVI / Cluster
Set Top Box	Base Stations	HUD / Telematics
Game Consoles	Access Points	Military / Aerospace
Digital Imaging		Robots / Drones

U8-Series

Scalable, Power-Efficient 64-Bit Microarchitecture for Embedded Intelligence

SiFive U8-Series

Design Goals for SiFive U8-Series Core IP

1.5X	2X	Class Defining
Performance Per Watt[1]	Area Efficiency[1]	Scalability

1- See Endnote For Details

SiFive U8-Series

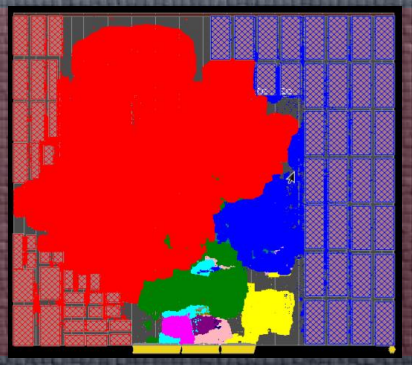
Delivering On The SiFive U8-Series Goals

Performance Per Watt	Area Efficiency	Scalability
SuperScalar	Tiny Area	Parameterized µArch
Out-Of-Order	Low Power	Composable Cache
10-12 Stage	Configurable	Optional FPU
Triple-Issue	Extensible	9-Core Mix+Match Cluster

SiFive U8-Series: RISC-V High Performance CPU

SiFive U84

2.63mm^2
Quad-Core CPU w/2MB L2$



0.28mm^2
CU Core without L2$

2.3X
Higher IPC[2]

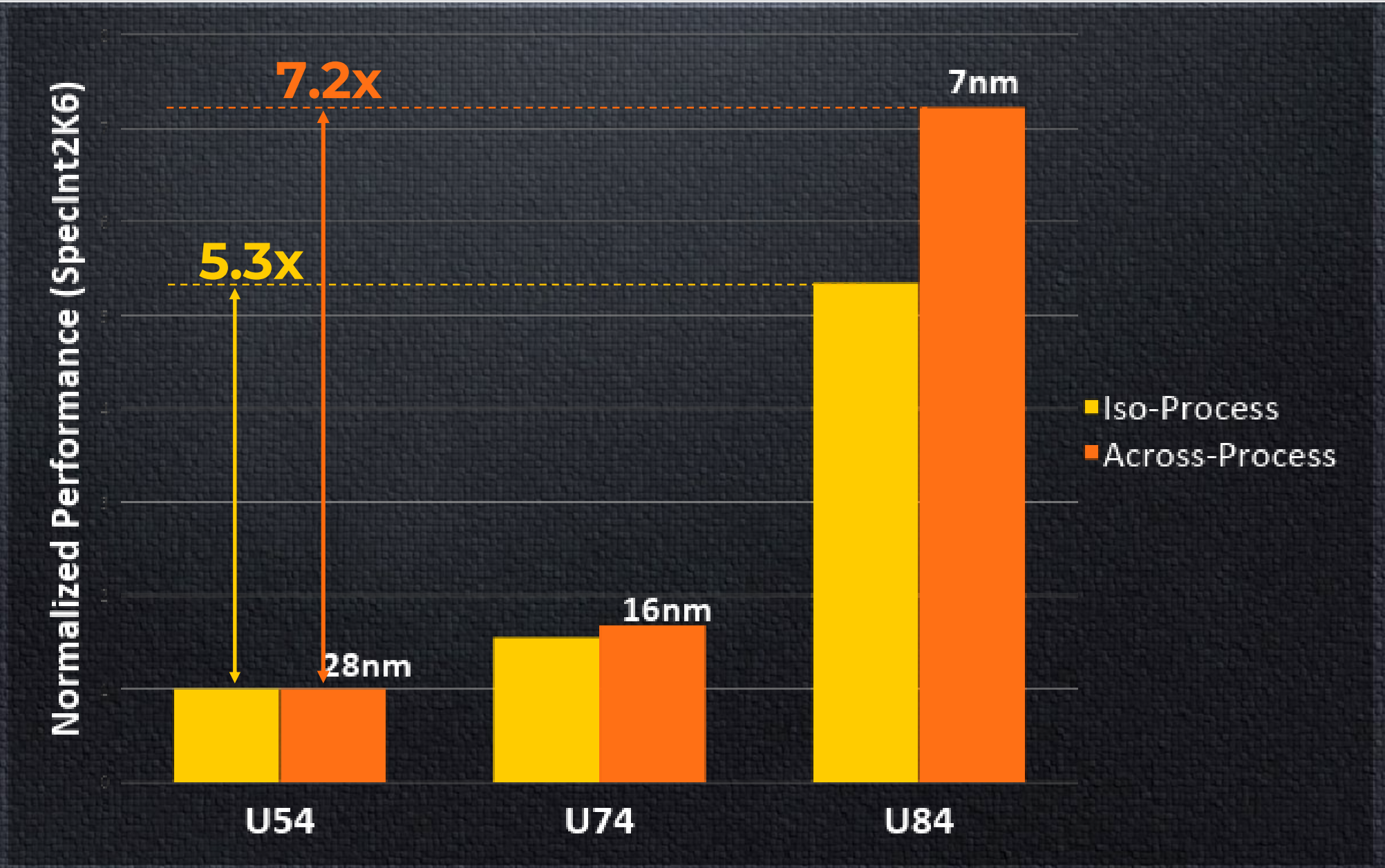
3.1X
Total Performance[2]

1.4X
Higher Frequency[2]

2.6GHz Frequency in 7nm

2- See Endnote For Details

U8-Series : Breakthrough Performance for RISC-V



SiFive U8-Series

Introducing U8-Class Processor Core IP

SiFive U84 A High-Performance Scalable 8-Series Core

SiFive U87 A High-Performance Scalable 8-Series Core with Vector Processing

Debug, Software, and Ecosystem

SiFive Debug

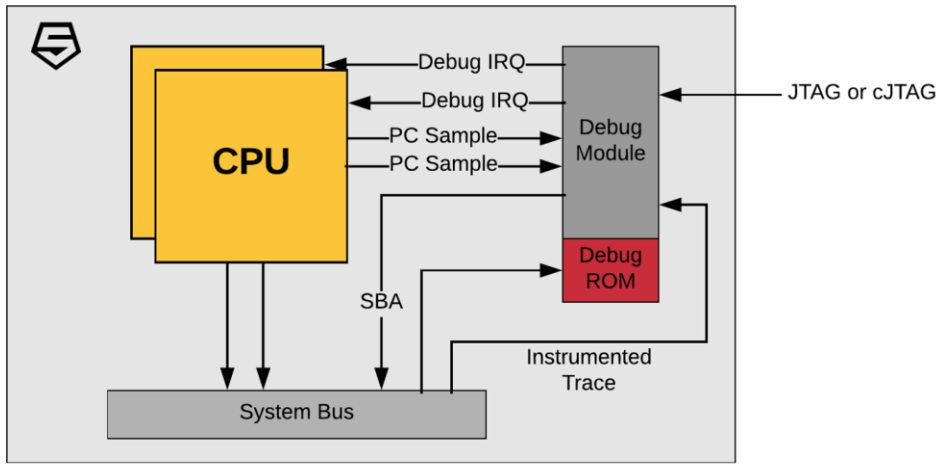
SiFive Debug IP

Access, Observe, Control

SiFive's Debug IP portfolio gives developers the power to efficiently debug SiFive based designs. From simple run control debug, to cross-triggering, to advanced multicore trace solutions, all delivered **pre-integrated** and **verified** together with SiFive's RISC-V Core IP in a single deliverable.

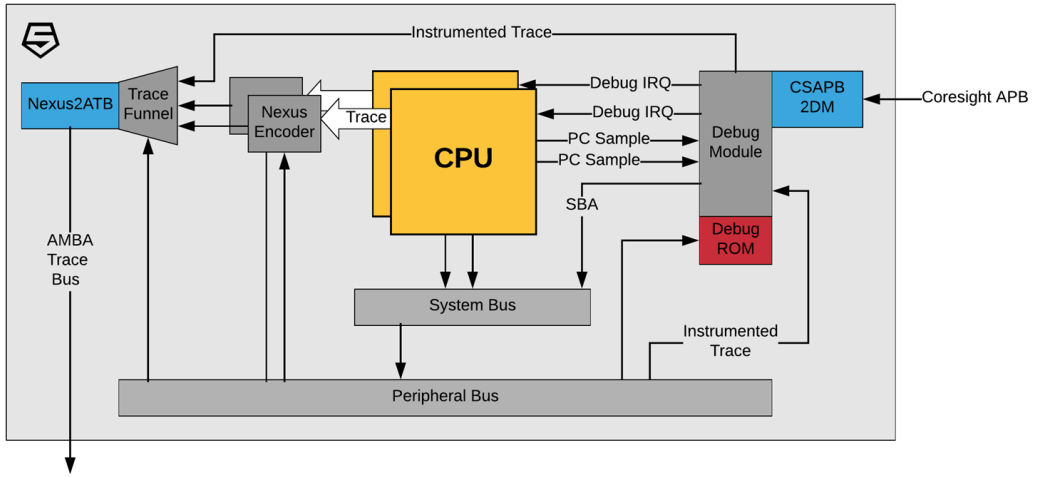
Basic Debug IP

Everything needed for run-control debug, and more.
Included with every Core IP subscription.



Advanced Debug IP

Enabling Nexus trace, advanced debug control, and Coresight compatibility.

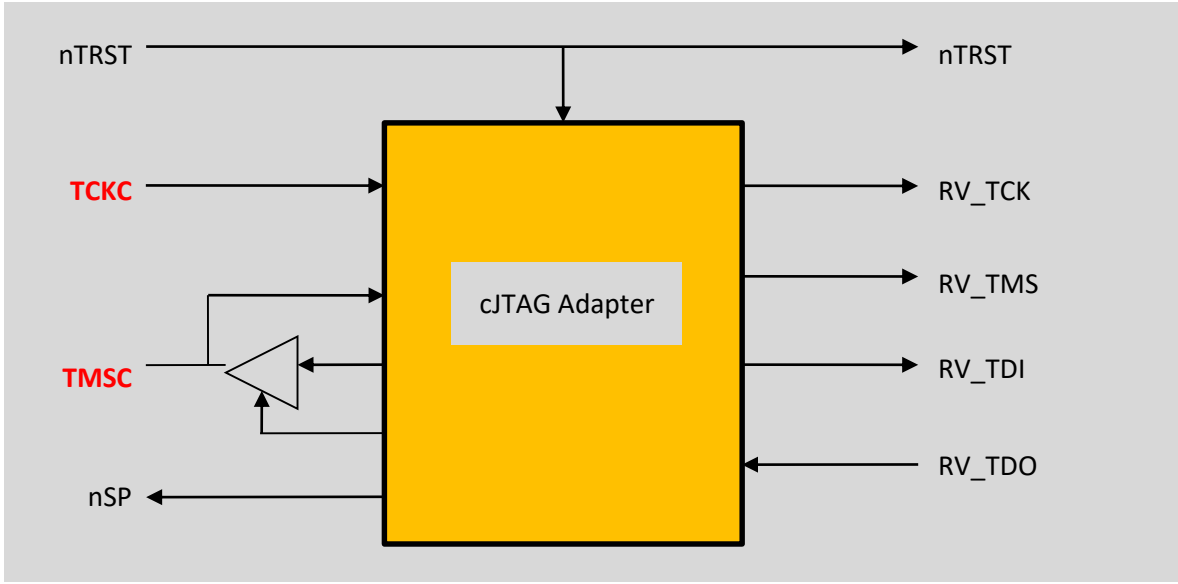


Debug Features - Available Now

- **Standard Run Control – go, halt, single step by instruction**
  - When halted by probe or external trigger, core takes a debug interrupt and begins execution at 0x800
  - Software breakpoint: EBREAK instruction also causes execution to go to debug interrupt
  - s0 reg is copied to DSCRATCH reg; core then runs tight loop until GO or RESUME flags are set
- **Read/write registers and memory**
  - Fast mode for reading/writing blocks of memory
- **SBA – System Bus Access**
  - Optional, allows debugger to access memory directly without core intervention
  - Useful for periodic sampling of pertinent variables
  - Can be used to implement low overhead semi-hosting
- **Multi-hart and heterogeneous core debug control**
  - For multi-core, select hart (hardware thread) first (1 of up to 1024)
  - Hardware can be configured with up to 31 halt groups
  - Each group supports synchronous start, stop of all harts defined in group when any one enters debug mode
  - External trigger input/output pairs, go to periphery of core complex
    - Can configure 0 to 16 pairs
    - 2-wire request/acknowledge handshake (CoreSight CTI compatible), can cross clock boundaries
    - If trigger input asserted, will cause group of harts to enter debug mode
    - When hart group halts, external trigger out is asserted to a CTM (CoreSight cross-trig matrix) or customer logic

cJTAG Support: Available Now

- **Optional 2-wire IEEE 1149.7 (cJTAG) interface**
- **Classic JTAG run control debug with only 2-Wires**
  - Perfect for pin constrained designs
- **Fully supported by IAR iJet, Lauterbach, Olimex, and SEGGER JLINK probes**



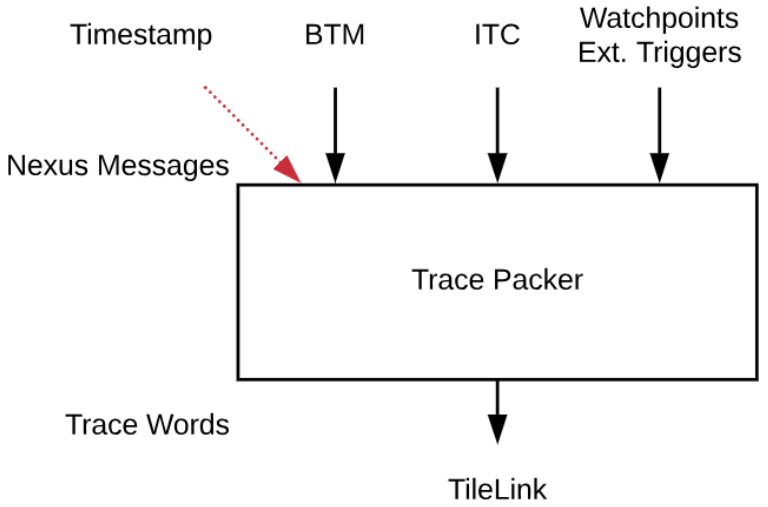
cJTAG System Block Diagram

Instruction Trace Features

- **Trace protocol based on Nexus standard**
  - IEEE-ISTO 5001 standard since 2003, expanded in 2012 for SERDES trace sink
  - Established standard, protocol includes message types for extensions and customization
  - Well supported by the tools ecosystem such as Lauterbach, Ashling, Green Hills
- **Instruction trace messages**
  - Compresses trace by capturing only changes in program flow, using BTMs – Branch Taken Messages
  - **Direct Branch:** records number of half-words executed (I-CNT) since last branch, for branches where the destination is statically known
  - **Indirect Branch:** for branches with destinations that are determined at runtime
  - **Synchronization:** records full address for destination of an interrupt, or periodically as reference for other branches
  - **Ownership trace**: Message generated when instrumented code writes to the memory-mapped ITC - Instrumented Trace Component
    - Primarily used to record RTOS task ID when a context switch occurs
- **Timestamp** (optional)
  - Choice of internal (fixed frequency) or external timestamp, synchronized to TLclock
  - Width is parameterizable, typically 40 or 48 bits
  - Each Nexus message can include timestamp, or turned off to save bandwidth

Extensions to Instruction Trace

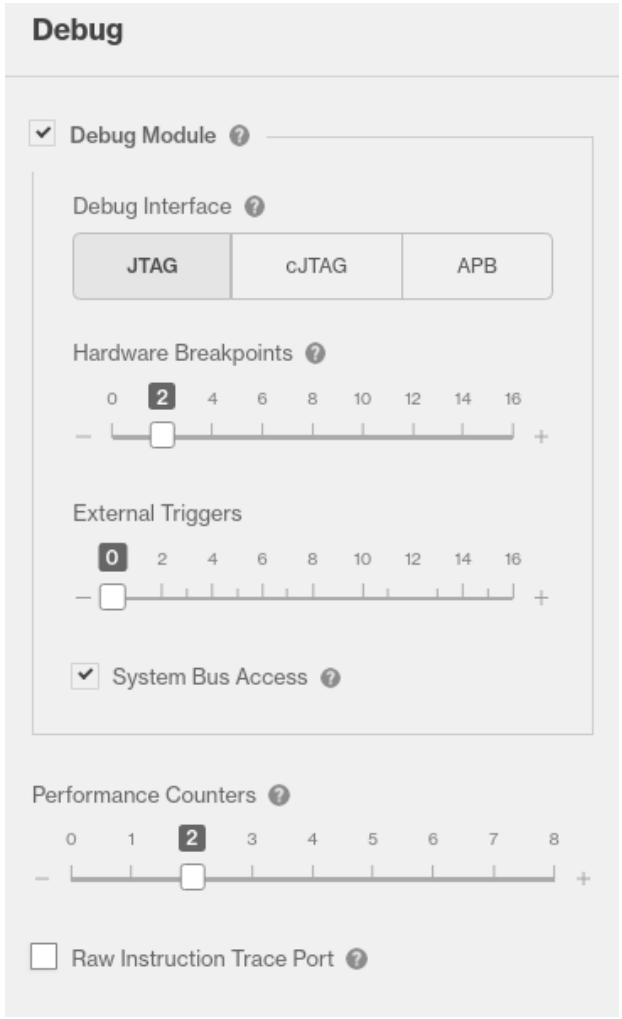
- **Multiple message sources**
  - **BTMs** – CPU instruction trace
  - **ITC –** Instrumented Trace Component (optional)
    - A set of memory-mapped Stimulus registers that, when written to, generate messages that includes register index + 32 bit data value
    - Writes are non-blocking
    - Supports byte, half-word, word writes
    - 32 mapped addresses; writes to upper half include a timestamp with the index and data written
  - **Watchpoints –** Core watchpoints
    - **Actions:** start trace, stop trace, insert Program Trace Sync message
    - **Edge mode** – transition from no-match to match; start or stop trace
    - **Range mode** – trace while watchpoint true, don't trace when false
    - **Use:** record markers in trace, w/ timestamp
      - Can be used for precise point-to-point timing of code
      - Watchpoints can also be variable address matches
  - **External Triggers**
    - Up to 8 external triggers supported for controlling trace
    - **Actions:** start or stop trace, record Program Trace Sync messages
      - Provides inserting markers into trace based on external events

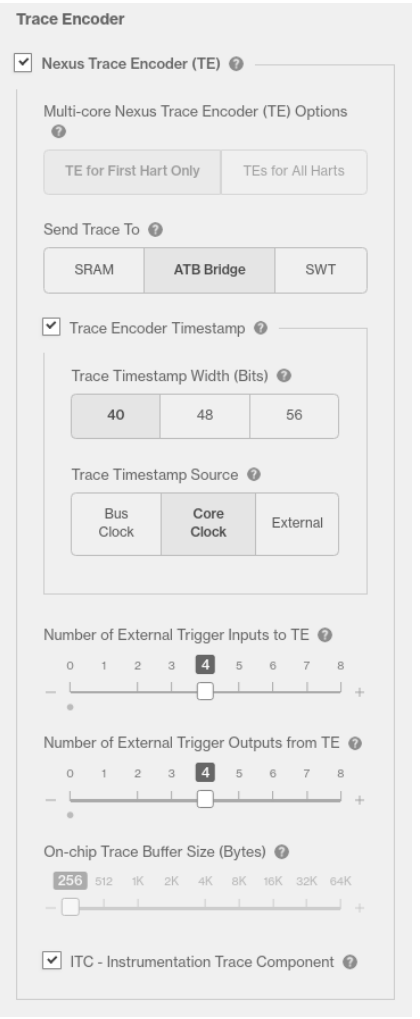


Trace Packer Merges Messages from Multiple Sources and Compresses the Data

Configured in SiFive Core Designer

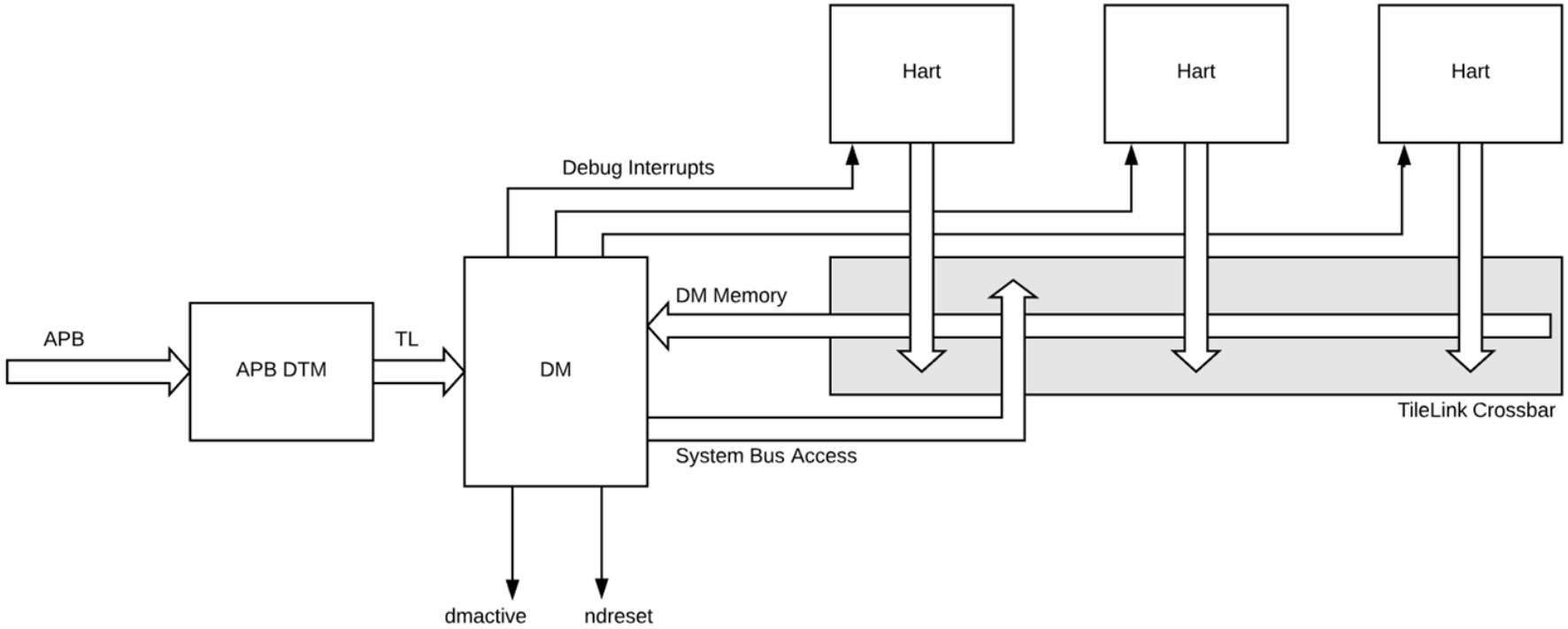
Pre-integrated and Verified alongside your Core IP using SiFive's cloud-based methodology





SiFive Debug: CoreSight Compatibility

- **APB DTM – APB Debug Transport Module is alternative to JTAG connection to Debug Module (DM)**
- **Allows ARM DAP to control SiFive cores**
- **User can insert an AXI or AHB-to-APB bridge if needed**
- **APB Debug Port occupies 4K bytes of APB memory space.**
  - DMI addresses are word granular so each register occupied 4 bytes in the APB space



Security

SoC Security Best Practices

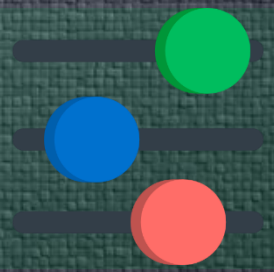
Replace Legacy Solutions

Reduce Trusted Computing Base

Clear Root-of-Trust

Auditable

Securing The RISC-V Revolution



Scalable Architecture

Multi-Core Privilege Modes
Per Memory PMP Regions

Greater Isolation

Per Core or Per PID Protection
H/W Bus Master Coverage

Finer Grain Controls

Per Peripheral Access Control

System-Level Security

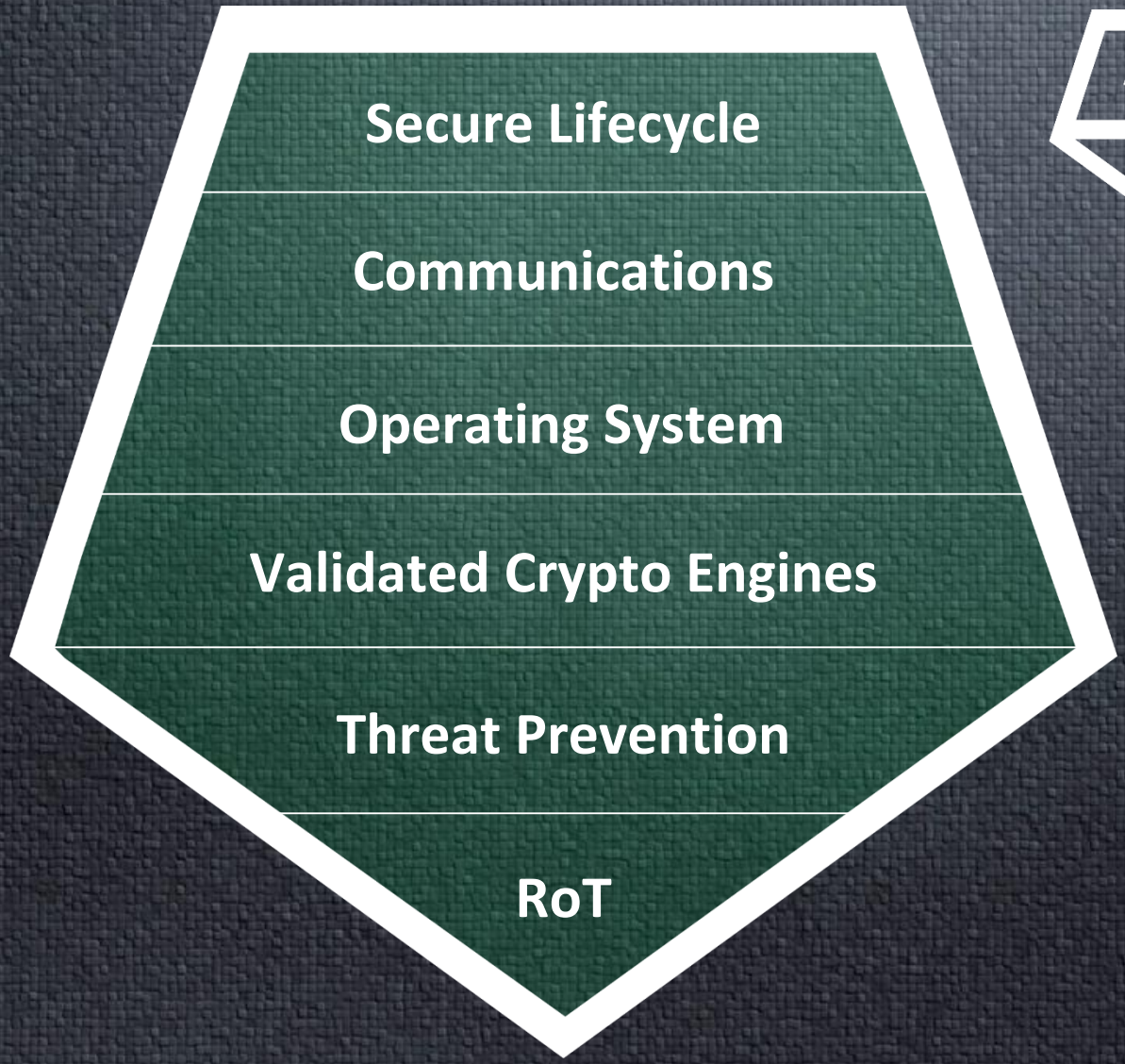
Unified Open Hardware and Software Security

SiFive Shield

The SiFive Open Secure Platform Architecture

Open Specification	Designed For Scalability	System Level Protection	Customizable

Implementing An Open, Scalable and Secure Platform



SiFiveShield

SiFive Shield – Multi-Domain Security

SiFive WorldGuard

A Fine-Grain Security Model for Isolated Code Execution & Data Protection

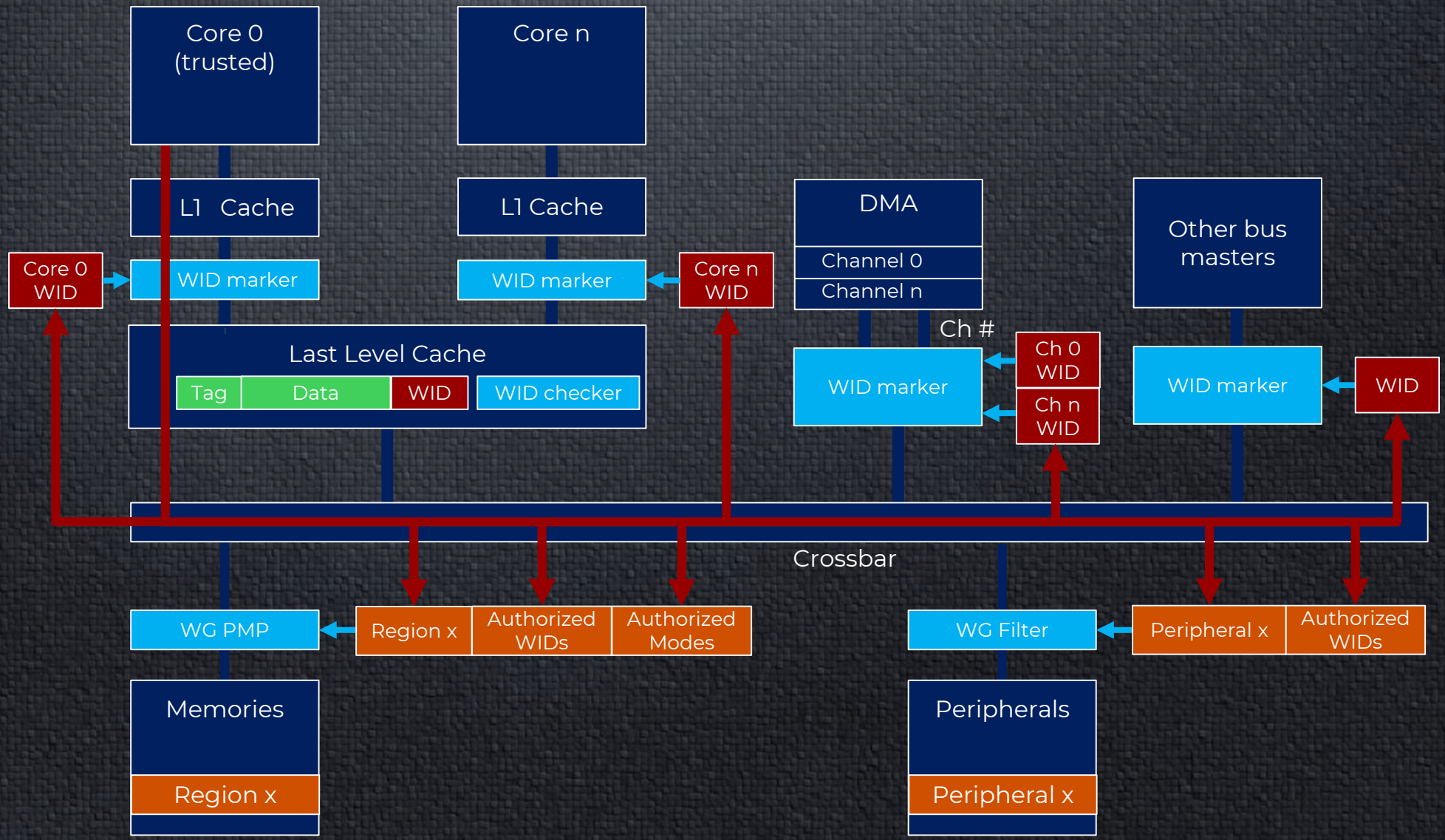
Multi-Domain Security Model with Fine Grain Control

SoC Level Information Control with Advanced Isolation Control

Data Protection For Core, Cache, Interconnect, Peripheral and Memory

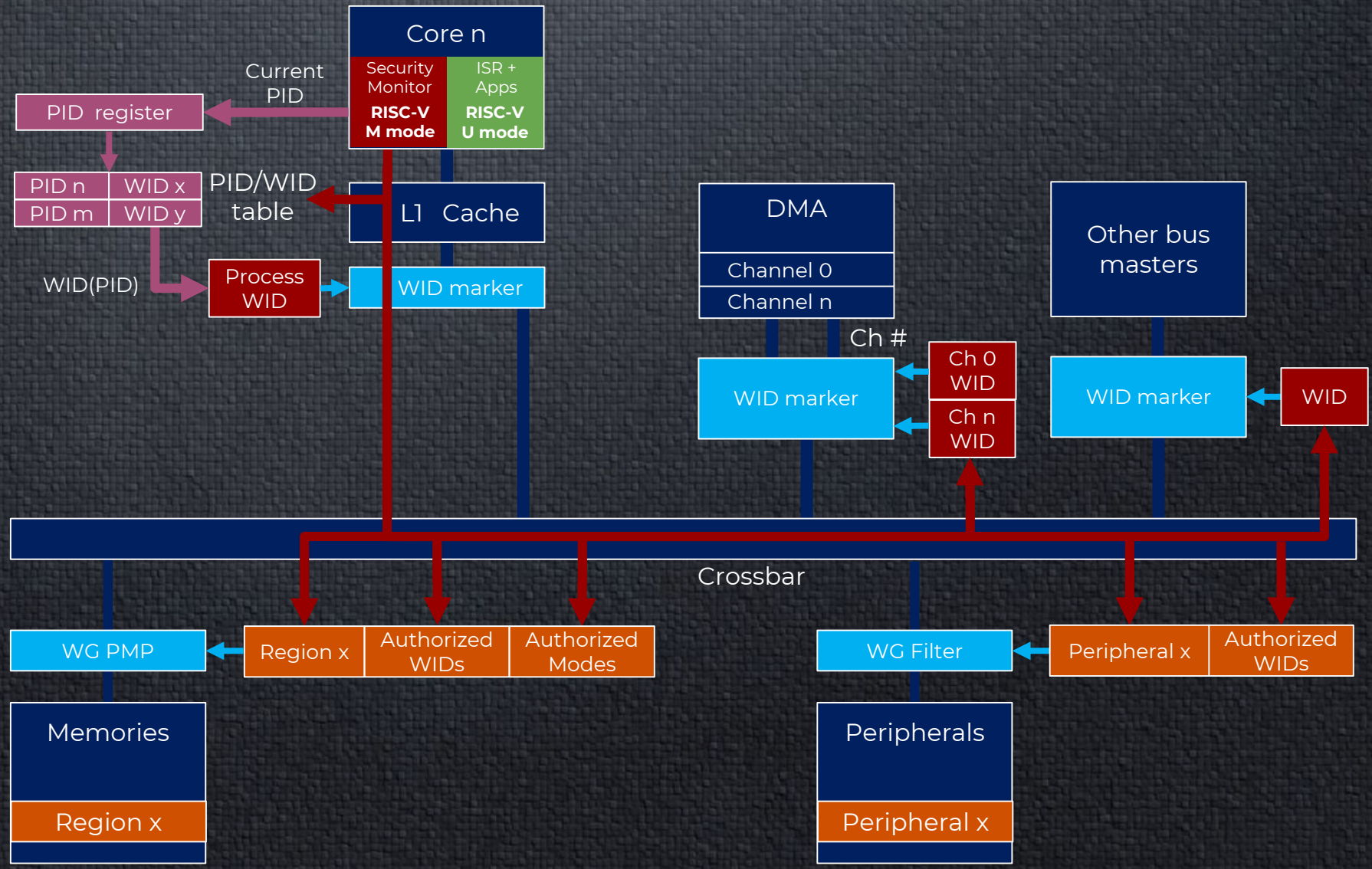
SiFive WorldGuard

Core Driven Mode for Multi-Domain Security



SiFive WorldGuard

Process Driven Mode for Multi-Domain Security



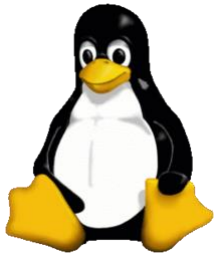
SiFive Shield

Feature	SiFive Shield	‘Competitive’ Solutions
Support for Multiple Worlds	Unlimited	Partial
Multi-Core Support	Yes	Partial
Software complexity	Low	Very High
Recompilation Requirement	None	Full
Full ISR in user mode	Yes (RISC-V)	No
Isolation per PID	Yes	No
DMA Protection	Yes	Yes
Memory & Peripheral Filter	Yes	Yes
In-house Crypto Engines	Yes	Yes
Key provisioning	SiFive Service (or 3rd Party)	3rd Party
Open Source Secure Boot	Yes	Yes

SiFive

Software and Ecosystem

RISC-V Open Source Tools Status

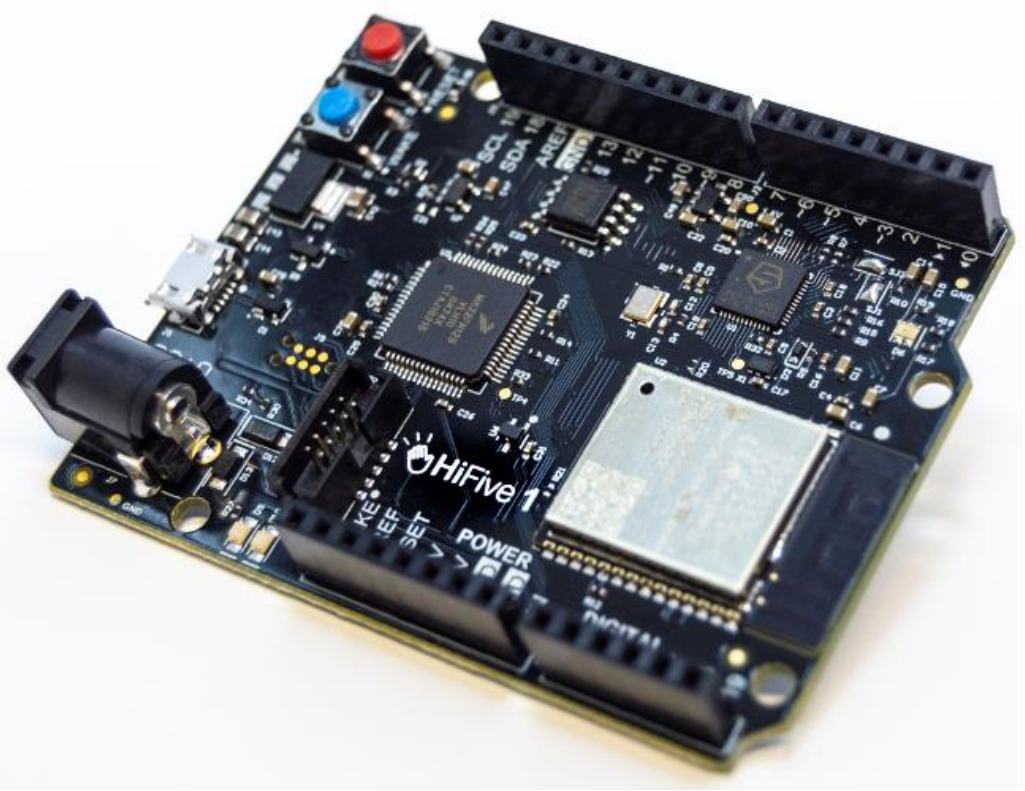


Software	Status	Recommended source release	Notes
GCC	Upstreamed as of 8.3	Upstream or SiFive: https://github.com/sifive/freedom-tools	SiFive maintains binary and source distributions which may contain patches which have not be upstream yet
LLVM	Upstreamed as of 9.0	https://github.com/llvm-mirror/llvm	Non-experimental support released as of version 9.0
GDB	Upstreamed as of 8.3	https://github.com/riscv/riscv-gnu-toolchain	
binutils	Upstreamed as of 2.32	Upstream	
newlib	Upstreamed as of 2.5.0	Upstream	
glibc	Upstreamed as of 2.27	Upstream	
Linux Kernel	Upstreamed as of 4.15 & 5.13	Upstream or SiFive: https://github.com/sifive/riscv-linux	
qemu	Upstreamed as of 4.2	Upstream	
OpenOCD	Not upstreamed	https://github.com/riscv/riscv-openocd	Upstreaming OpenOCD is planned, but low priority

SiFive

Embedded

HiFive1 Rev B: Embedded RISC-V Dev Board



- SiFive FE310-G002 (built in 180nm)
- Operating Voltage: 3.3 V and 1.8 V
- Input Voltage: 5 V USB or 7-12 VDC Jack
- IO Voltages: 3.3 V only
- Digital I/O Pins: 19
- PWM Pins: 9
- SPI Controllers/HW CS Pins: 1/3
- Hardware I2C: 1
- UART: 2
- External Interrupt Pins: 19
- External Wakeup Pins: 1
- Flash Memory: 4 MB Quad SPI
- Host Interface (microUSB): Program, Debug, and Serial Communication

Order on Crowdsupply

SiFive Embedded Software Ecosystem

- **SiFive Freedom Studio**
  - Eclipse CDT, GNU MCU Eclipse, pre-built GCC, and OpenOCD
  - Built on Open Source technology
- **SEGGER -** JLINK Probe and Embedded Studio RISC-V IDE
- **Lauterbach -** Lauterbach TRACE32 for silicon bring up and debug
- **IAR -** IAR Embedded Workbench with SiFive support in development
- **Ashling -** RiscFree C/C++ IDE for development and debug
- **Embedded Operating Systems**
  - FreeRTOS
  - Zephyr OS
  - RTEMS
  - Express Logic – Thread X
  - Micrium - µCOS
  - RIOT
  - NuttX
- **Imperas -** Simulation models and tools for early software development

Freedom Studio

SEGGER

IAR SYSTEMS

LAUTERBACH DEVELOPMENT TOOLS

expresslogic

imperas

Zephyr™

ASHLING

RIOT

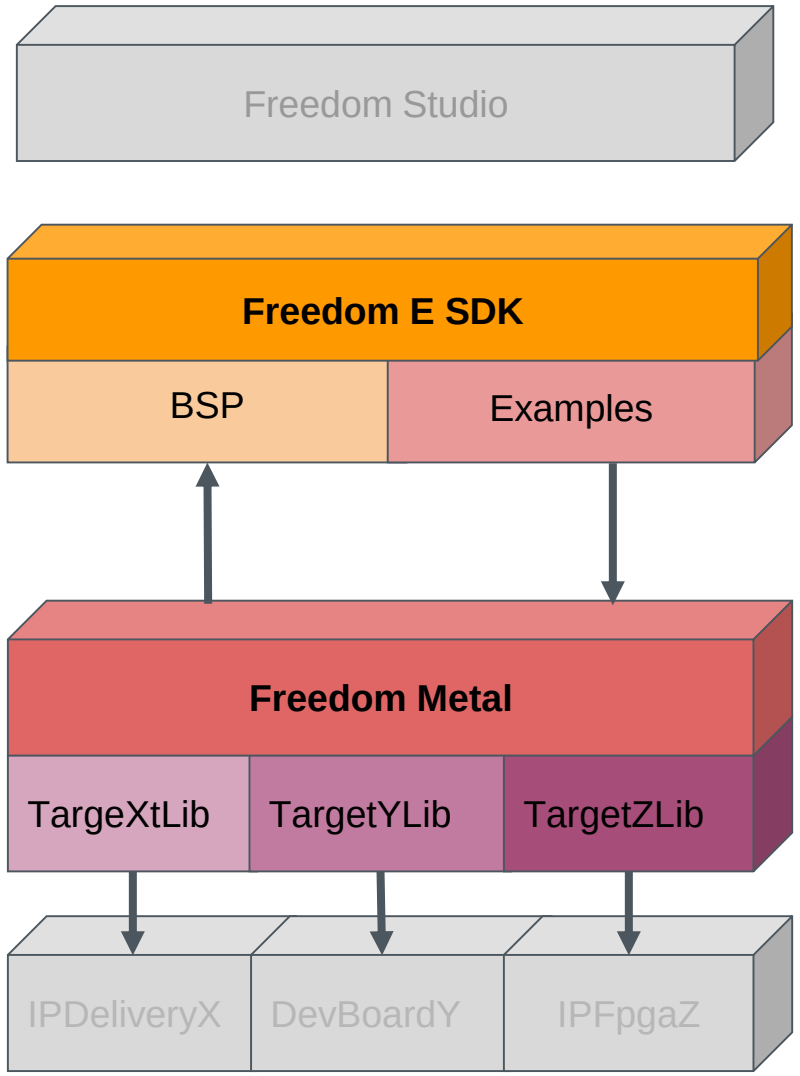
Freedom E SDK & Metal - A Bare Metal SW Stack for SiFive Devices

What is Freedom E SDK

- Embedded development kit providing a command line driven workflow with Examples, FreeRTOS, and Utilities
- Freedom Metal BSPs are available for all SiFive Deliverables
  - IP Deliverables
  - Standard Core IP Deliverables
  - Standard Core FPGA Deliverables
  - SiFive Development Boards
- Examples use Freedom Metal to provide portability
- Open source repository
  - https://github.com/sifive/freedom-e-sdk

What is Freedom Metal

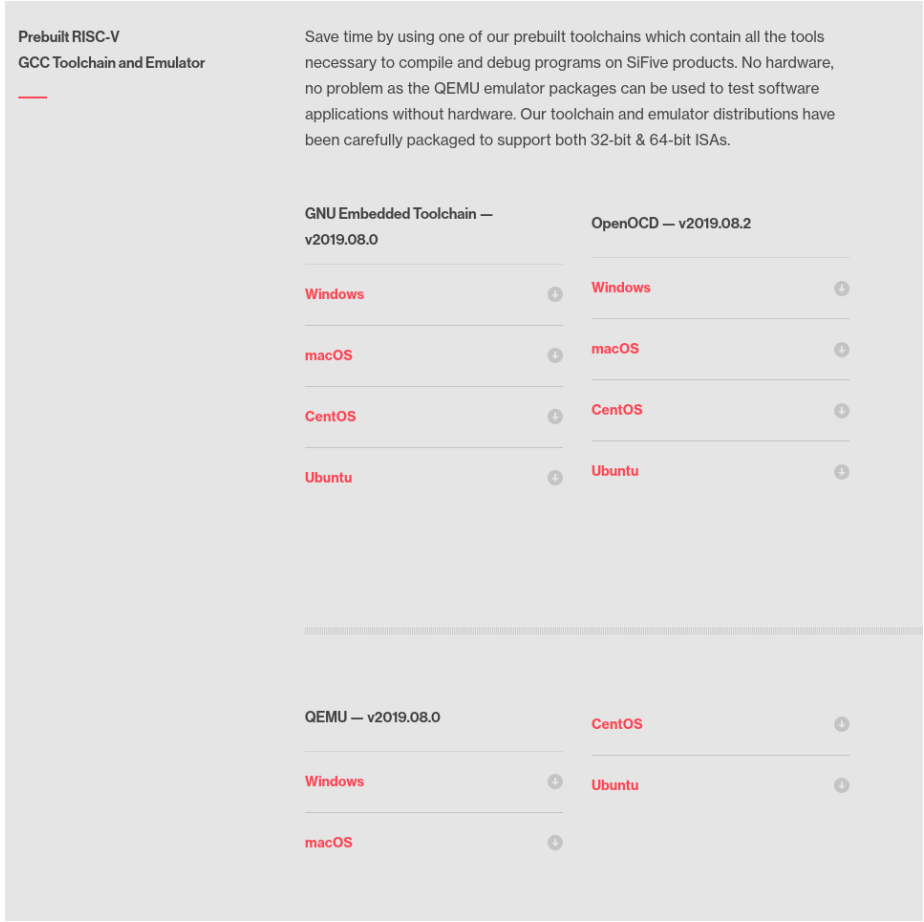
- Library for writing Portable, Bare Metal SW for all SiFive devices
  - A Bare Metal C application environment
  - An API for controlling CPU features and peripherals
  - The ability to retarget to any SiFive RISC-V product
  - A RISC-V hardware abstraction layer (HAL)
- Uses BSP's to provide target adaptation
- Open source repository
  - https://github.com/sifive/freedom-metal



SiFive Q3 Toolchain Update

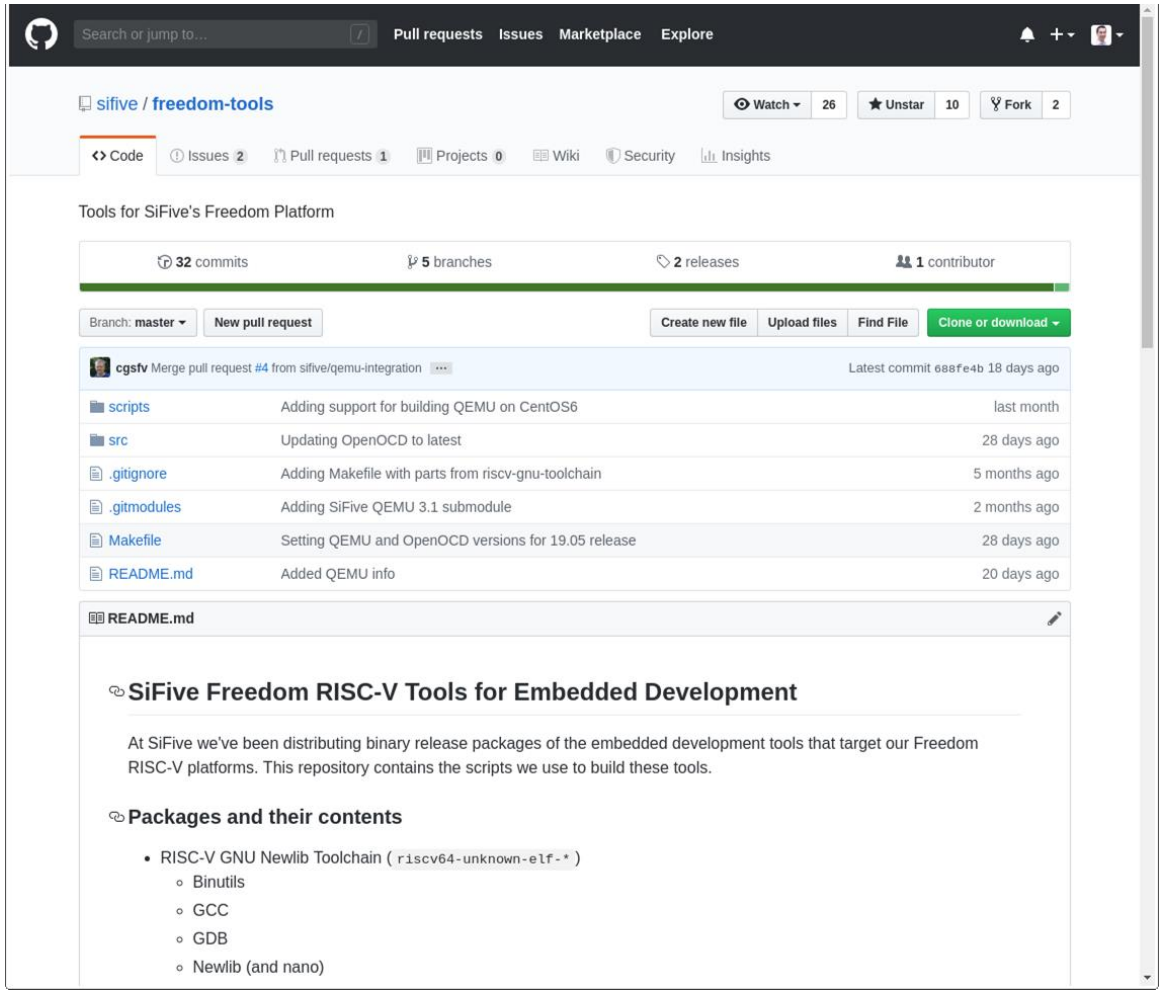
- **SiFive releases a new toolchain distribution every quarter**
  - Quarterly releases support
  - binaries - www.sifive.com/boards
  - source - https://github.com/sifive/freedom-tools

- **Features of SiFive's Toolchain Distribution**
  - GCC (newlib/newlib-nano)/GDB/QEMU
  - Support for all SiFive Core Designer generated cores
  - Enhanced support for SiFive IP
    - Pipeline tuning options for SiFive cores (eg: *-mtune=sifive-7-series*
    - CLIC Vectoring Mode Support (eg: *__attribute__((interrupt("SiFive-CLIC-preemptible"))));*)

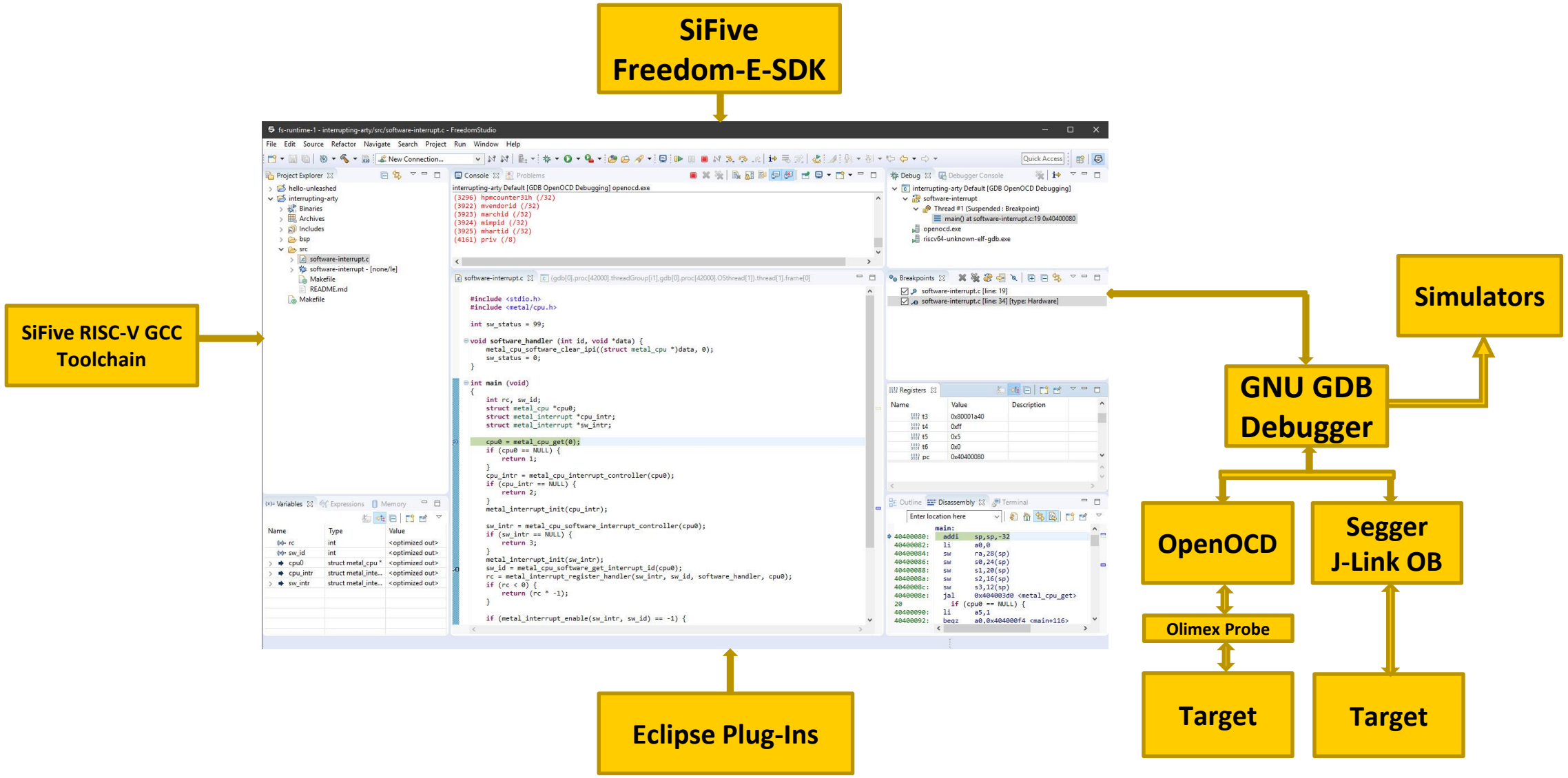


Freedom Tools

- **Sources and Build Scripts for all of SiFive's embedded toolchain's, debuggers, and Utilities**
- **RISC-V GNU Newlib Toolchain (GCC)**
  - Binutils
  - GCC
  - GDB
  - Newlib and Newlib-nano
- **RISC-V OpenOCD Debugger**
  - OpenOCD and necessary drivers for FTDI devices
- **QEMU Open Source emulator**
  - targets for both RV32 and RV64



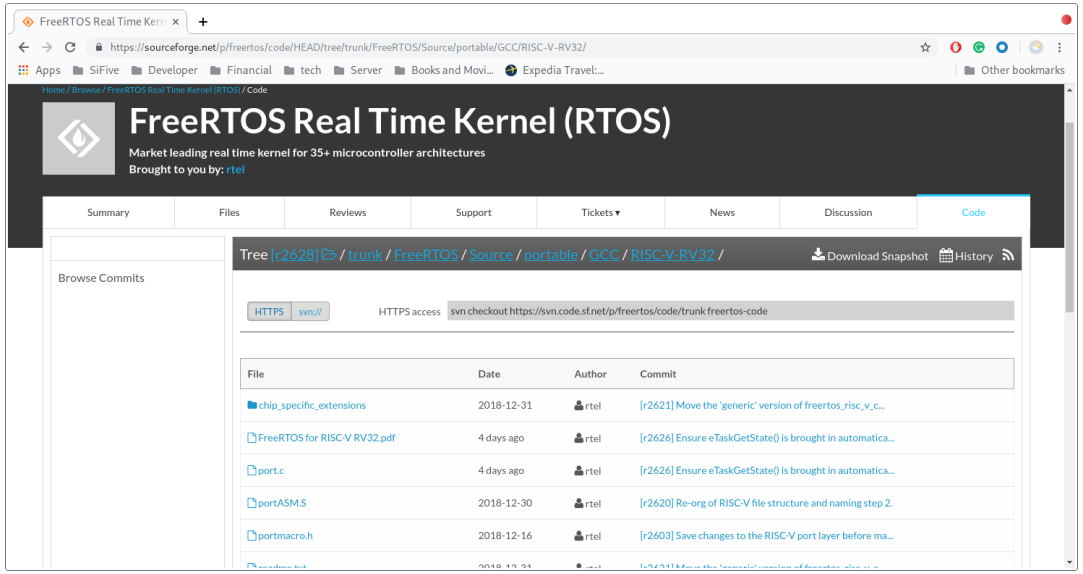
SiFive Freedom Studio



FreeRTOS - Delivered by SiFive

- **RISC-V officially supported as of FreeRTOS 10.2 (Feb 2019)**
  - 10.2.1 adds support for RV64
  - SiFive QEMU example included in the distribution

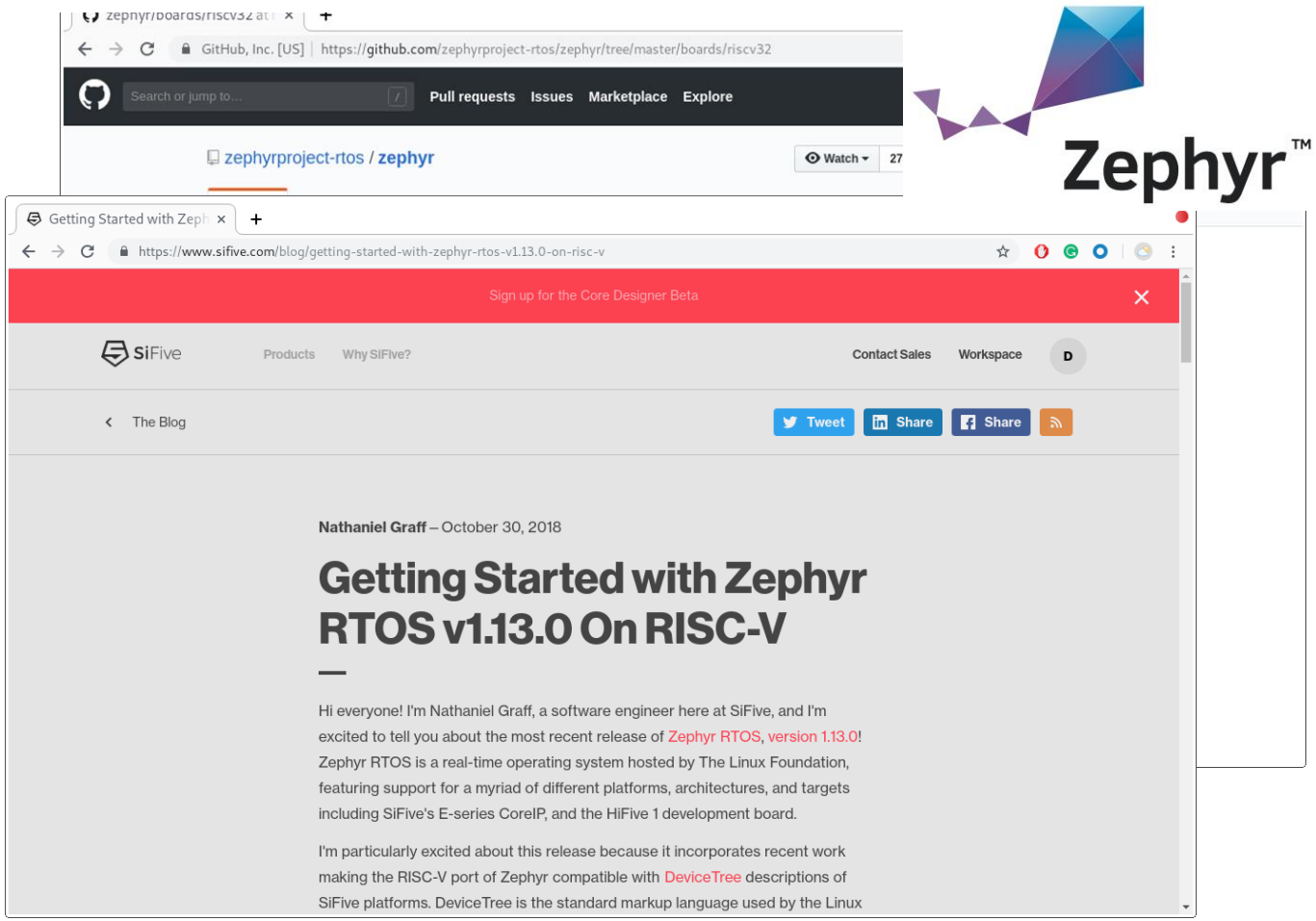
- **SiFive have created a FreeRTOS port to Freedom Metal for support for SiFive devices**
  - Generic support for all SiFive cores and tested against SiFive development platforms like the HiFive 1 Rev B
  - FreeRTOS examples added to Freedom E SDK and Freedom Studio



Zephyr - SiFive HiFive1 is Upstream and Well Supported

- **Zephyr RTOS**
  - Open Source
  - Well defined development cycle
  - Performant and scalable
  - Strong software stacks

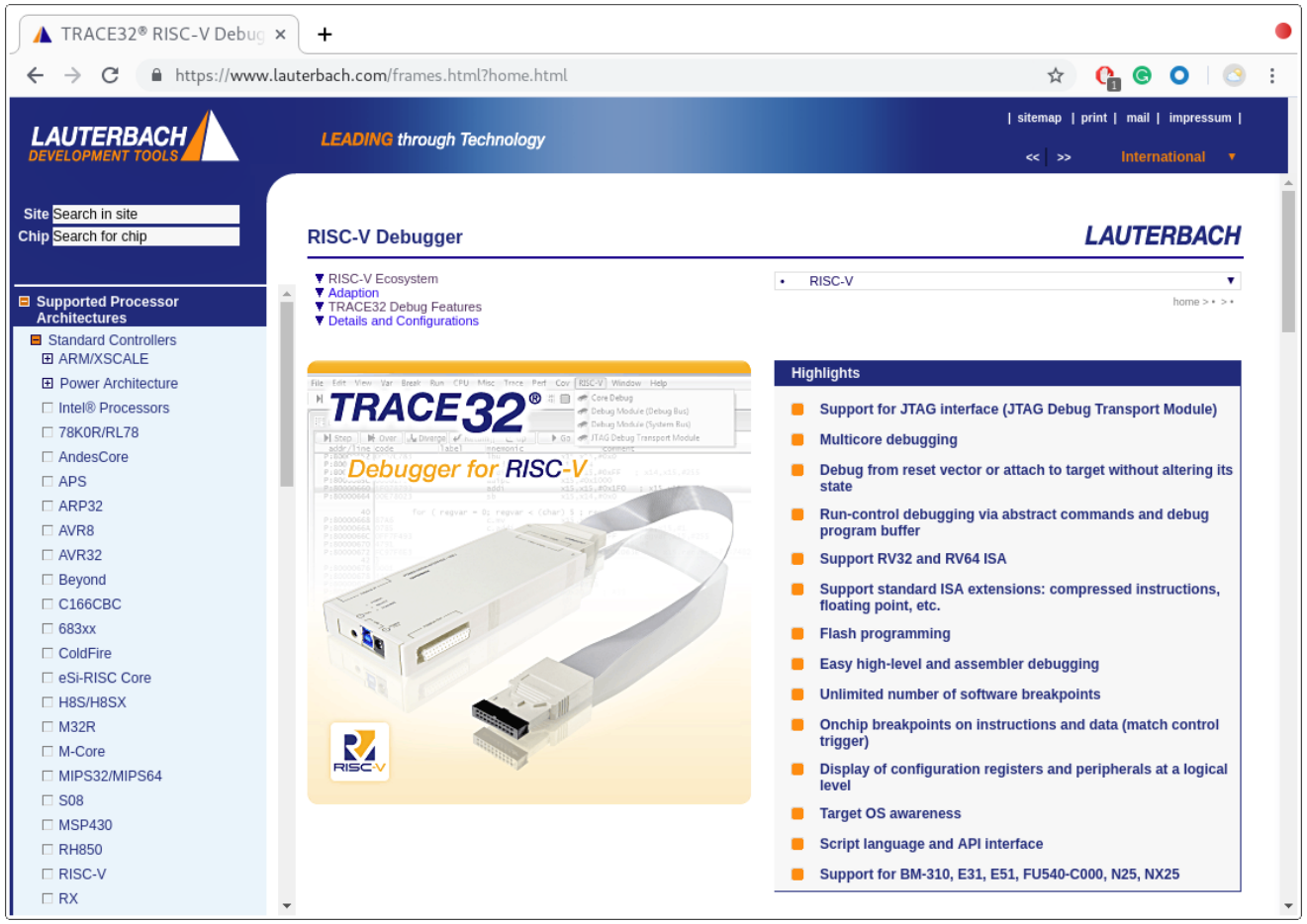
- **SiFive Zephyr Support**
  - HiFive1 Rev B board supported in the latest Zephyr LTS release



https://www.sifive.com/blog/getting-started-with-zephyr-rtos-v1.13.0-on-risc-v

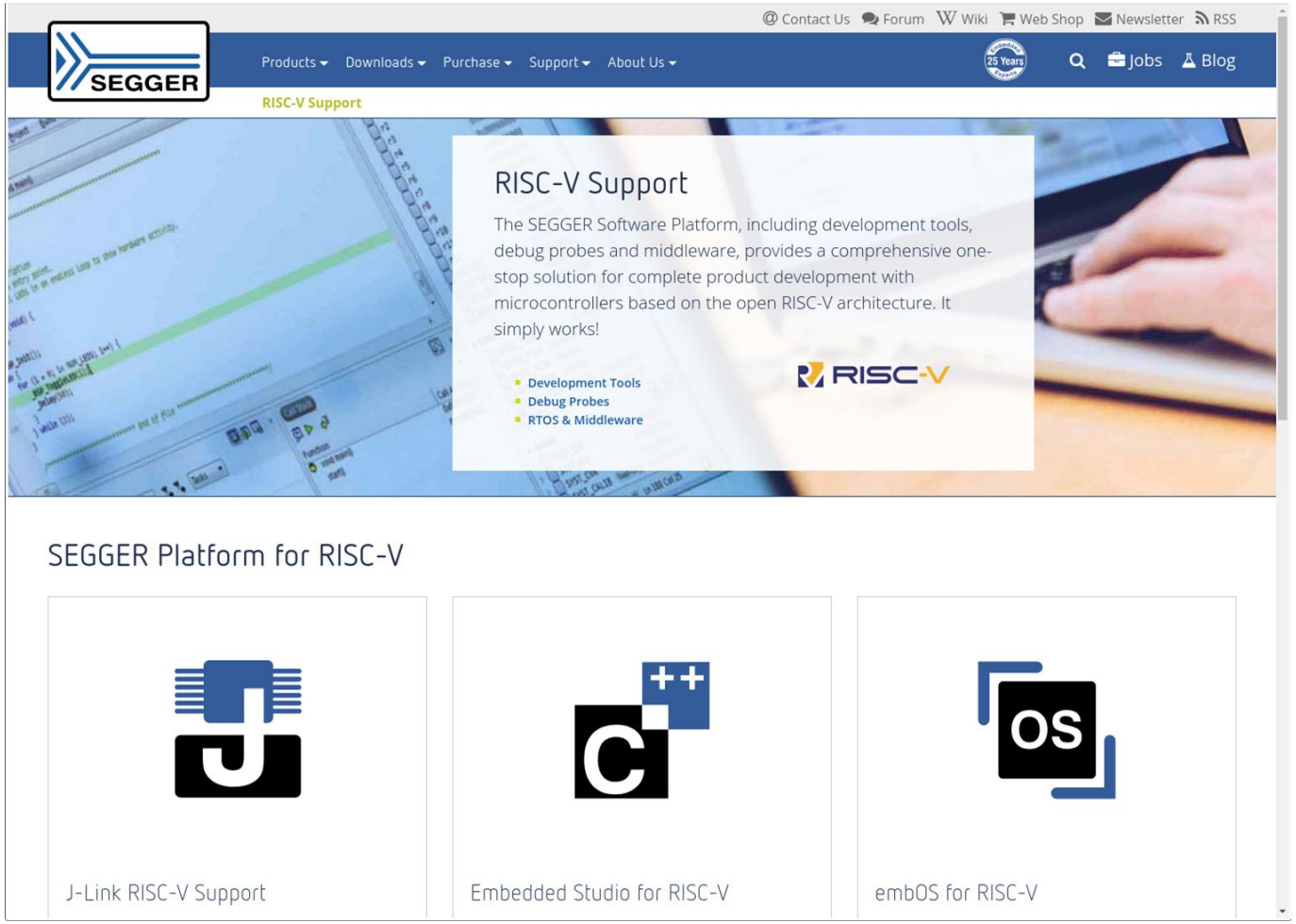
Lauterbach

- **Commercial RISC-V Debug Hardware and Software**
  - Available in the market for over a year
- **Support for all SiFive IP and platforms**
  - RV32/RV64
  - Multicore
  - Heterogeneous Multicore



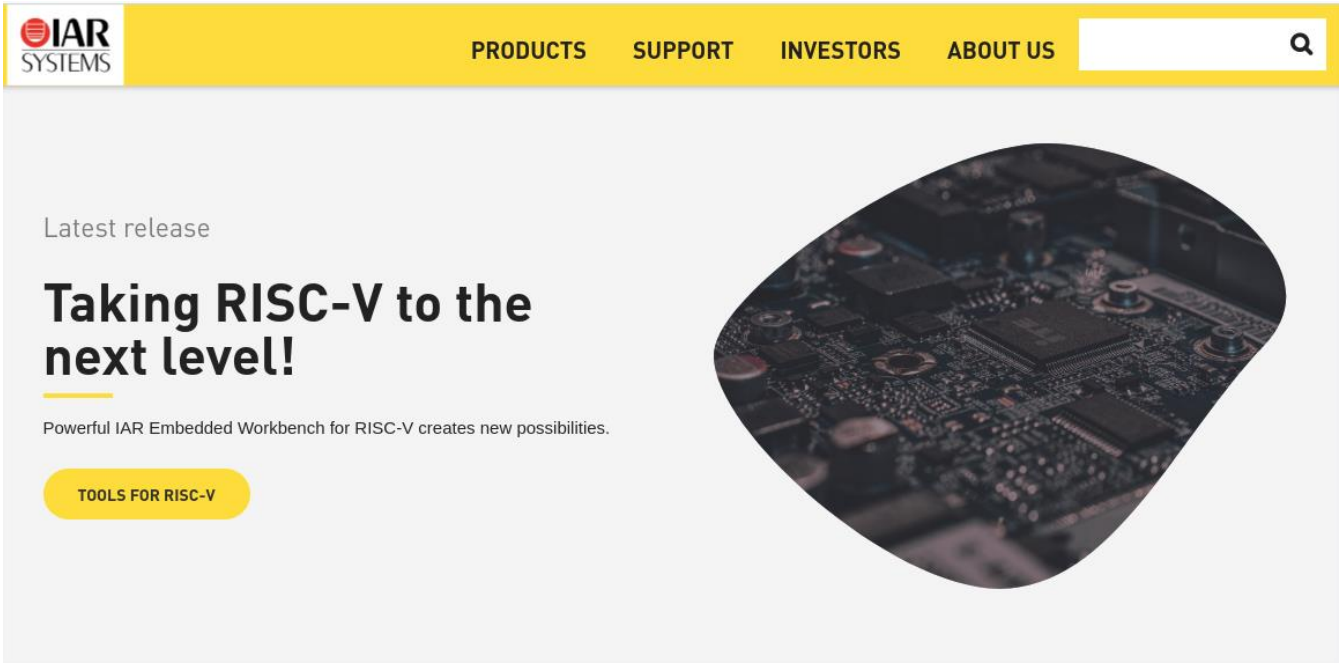
SEGGER

- **Commercial RISC-V Debug Hardware and Software**
  - Available since late 2017
- **Support for all SiFive IP and platforms**
- **SEGGER RTT fully supported**
  - High Speed communication with host debugger



IAR

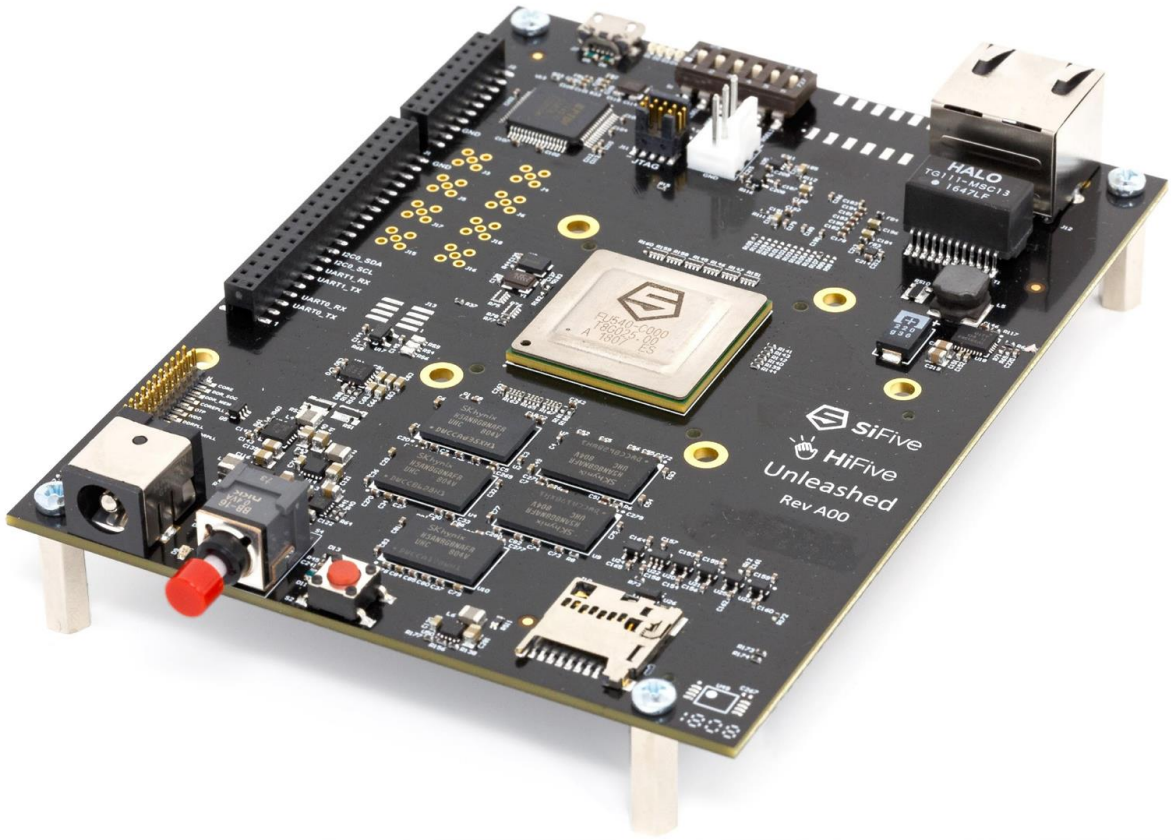
- **Very well known in the Embedded Space**
  - Have been around for a long time 20+ years
  - Support many different architectures
- **Known for embedded toolchain**
  - The first proprietary RISC-V Compiler
  - High-Quality compiler generating both good code Density and Performance



SiFive

Linux

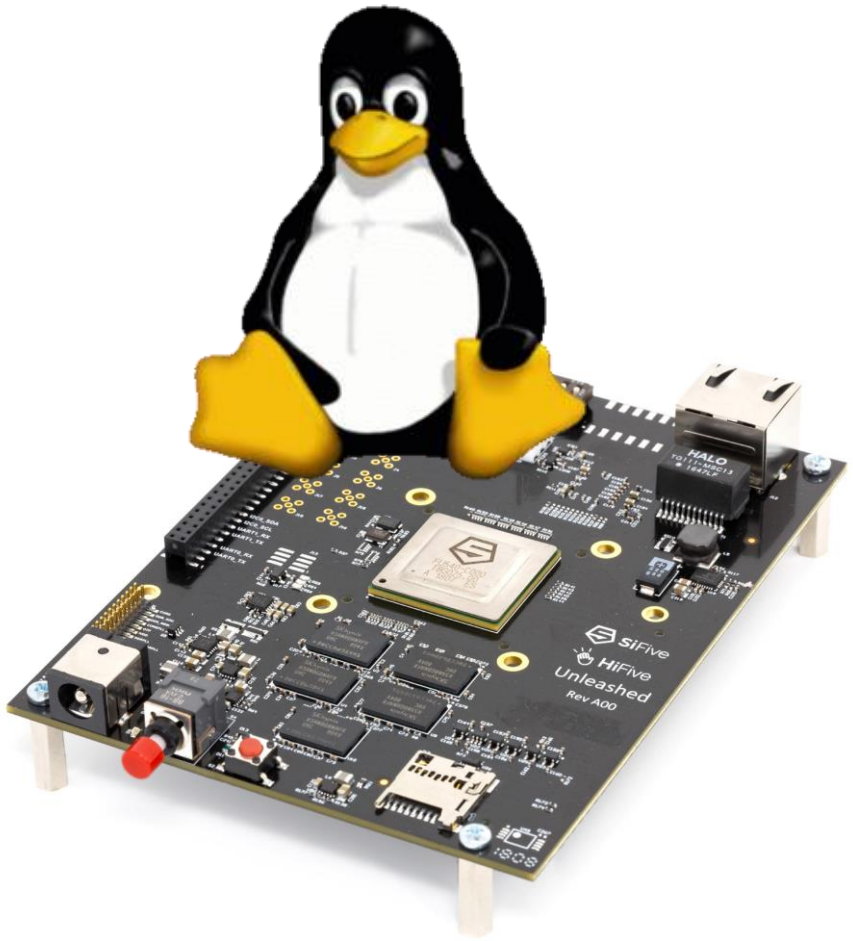
HiFive Unleashed: World's First Multi-Core RISC-V Linux Dev Board



- SiFive FU540-C000 (built in 28nm)
- 8 GB 64-bit DDR4 with ECC
- Gigabit Ethernet Port
- 32 MB Quad SPI Flash
- MicroSD card for removable storage
- MicroUSB for debug and serial communication
- Digital GPIO pins
- FMC connector for future expansion with add-in cards

Order now at crowdsupply.com for $999

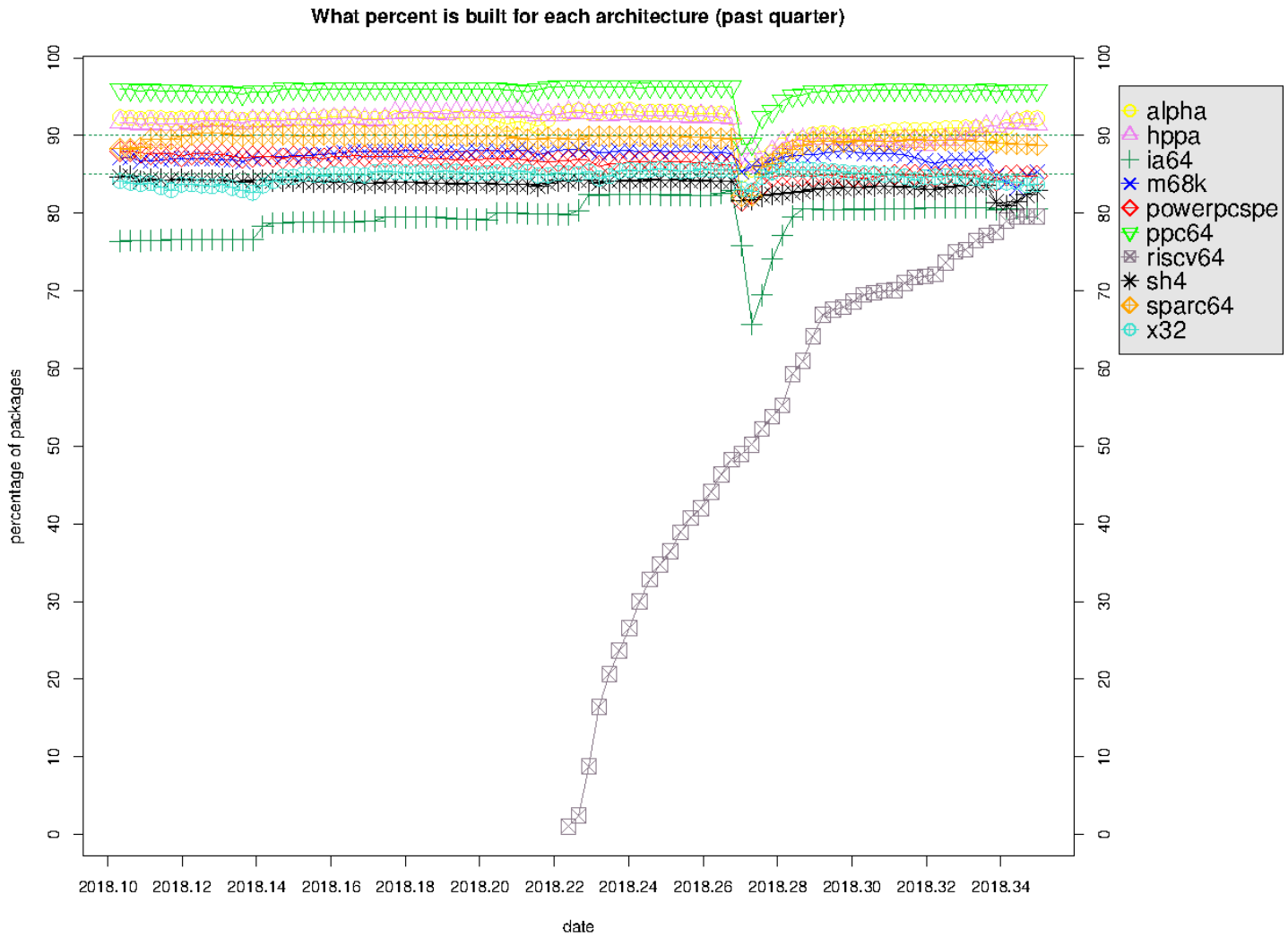
SiFive Linux Platform Enablement - uboot and YOCTO



- **SiFive engineers working on uboot and Yocto support for SiFive devices**
- **Uboot supporting existing HiFive Unleashed development boards available**
- **Yocto/Open Embedded BSP now abailable**
  - See Freedom-U-SDK
    https://github.com/sifive/freedom-u-sdk

Linux Distributions - Early Support

Debian Distro Package Build Status



RISC-V Debian Port Goals

- Software-wise, this port will target the Linux kernel
- Hardware-wise, the port will target the 64-bit variant, little-endian

80% of all Debian packages are ported as of today

Debian Distro runs on the HiFive Unleashed development board with the SiFive Freedom U540 SoC