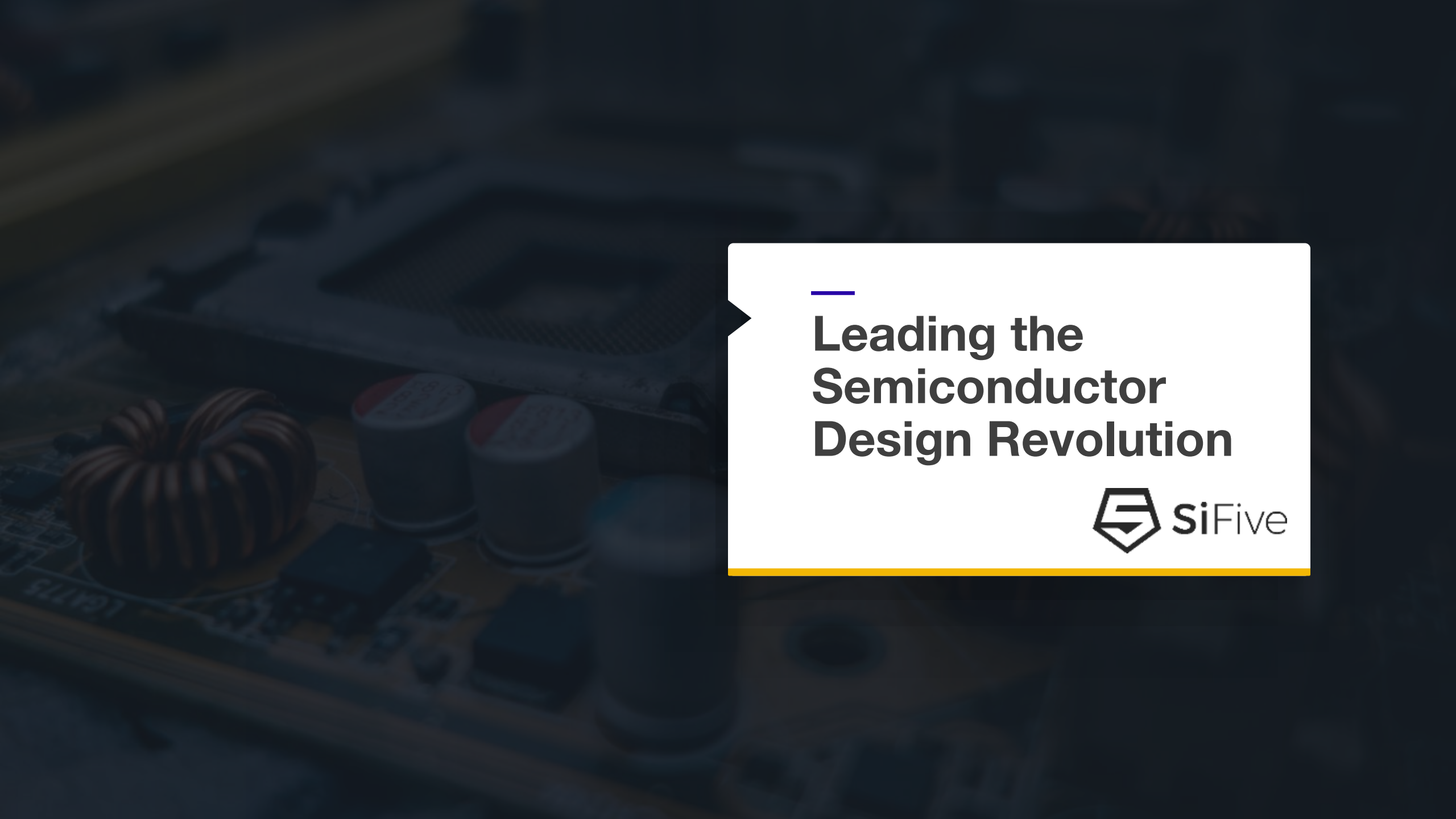
SiFive Tech Day

Hsinchu | Nov.14

SiFive



Leading the Semiconductor Design Revolution

SiFive

SiFive - Global Presence and Reach

World Class Expertise

- Inventors of RISC-V
- Chip Design in the Cloud
- RTL, PD, Silicon
- Design Platforms

SiFive Worldwide Presence

- 15+ Offices
- 550+ Employees
- 300+ Tapeouts

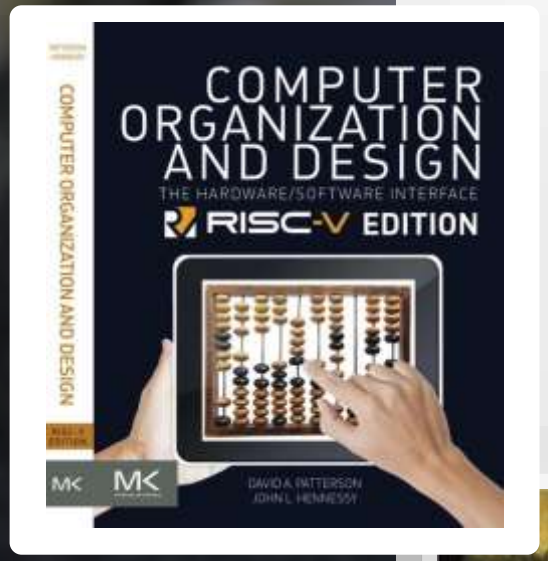
The RISC-V Revolution

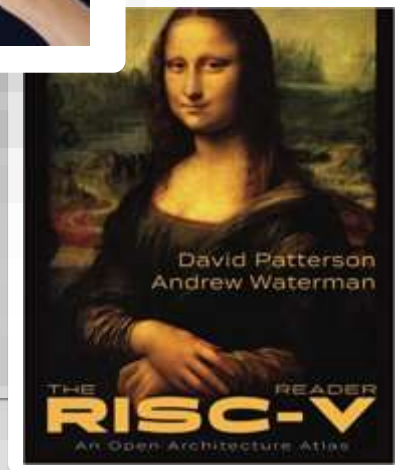
November 2019

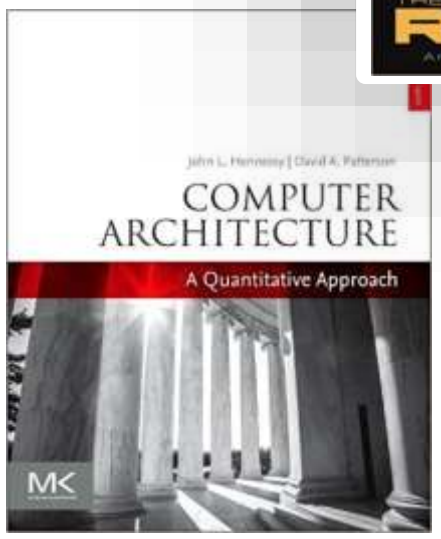
SiFive

SiFive

Academic
Adoption





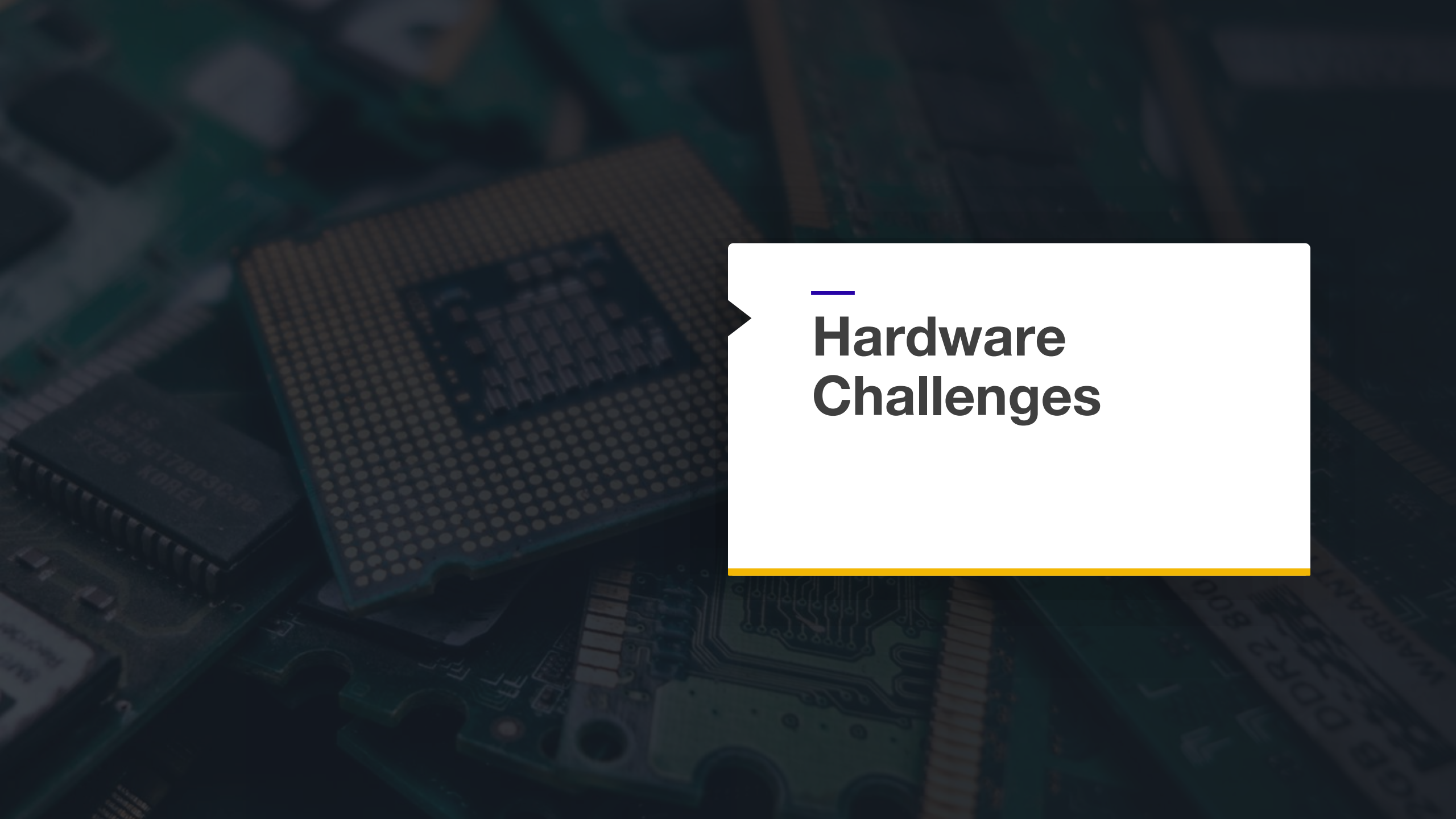


- RISC-V architecture and implementation are already taught/researched at UC Berkeley, Stanford, MIT, Technion and other top universities
- The next cohorts of engineers will enter the job market knowing RISC-V

Industry and National
Adoption

- ISA appropriate for all levels of computing systems, from MCU's to supercomputers
- Large companies are adopting RISC-V for deeply embedded controllers in their SoCs
- >35 silicon companies have embraced RISC-V
- NVIDIA has publicly announced that all future GPUs will use RISC-V
- Western Digital publicly announced their transition of all 1 billion+ cores per year to RISC-V
- India has adopted RISC-V as its national ISA
- US DARPA has mandated RISC-V in recent security proposals

RISC-V Ecosystem Momentum: Phenomenal

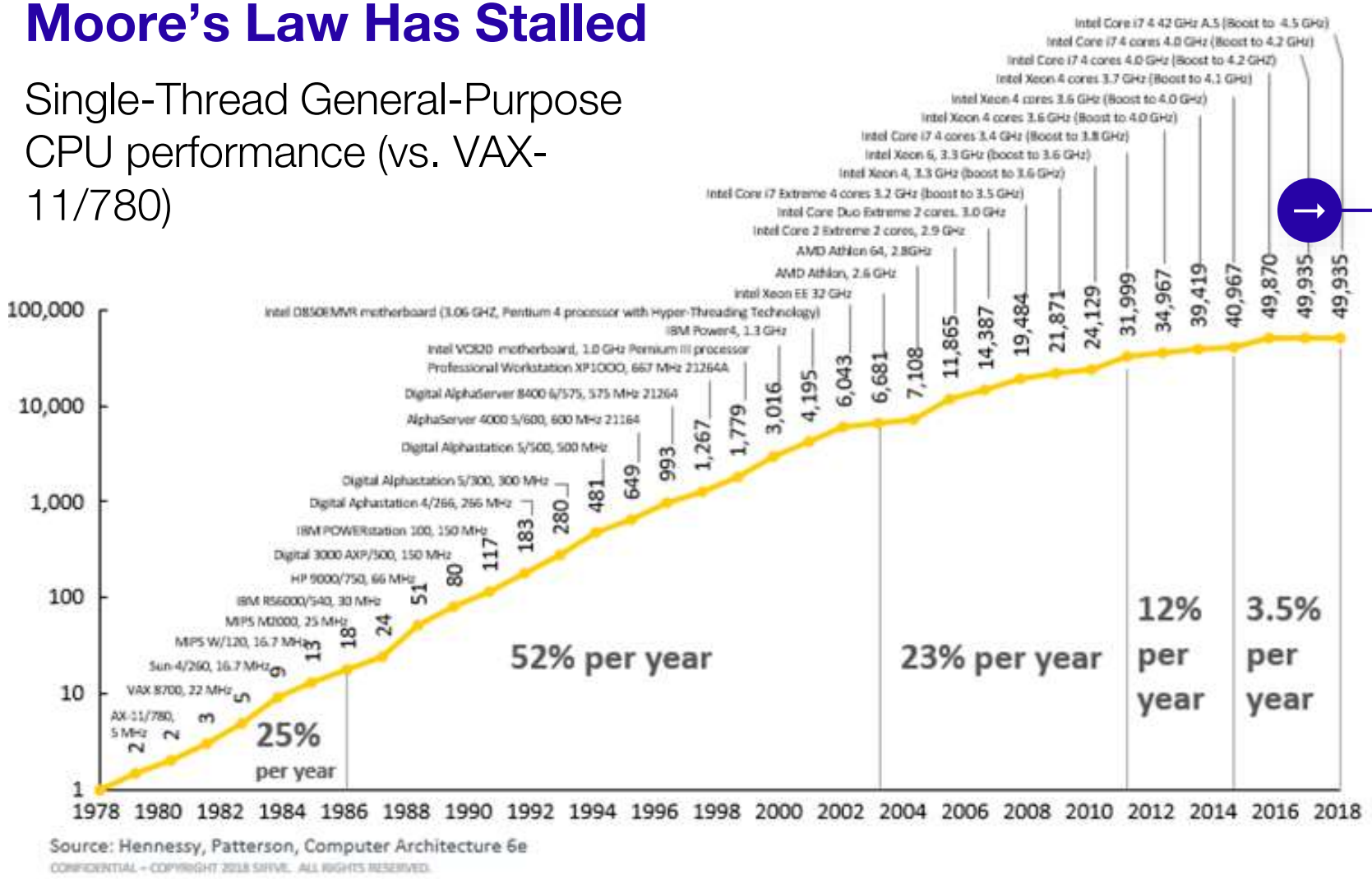


Hardware Challenges

Why RISC-V? Customization and Verticalization!

Moore's Law Has Stalled

Single-Thread General-Purpose CPU performance (vs. VAX-11/780)



Source: Hennessy, Patterson, Computer Architecture 6e

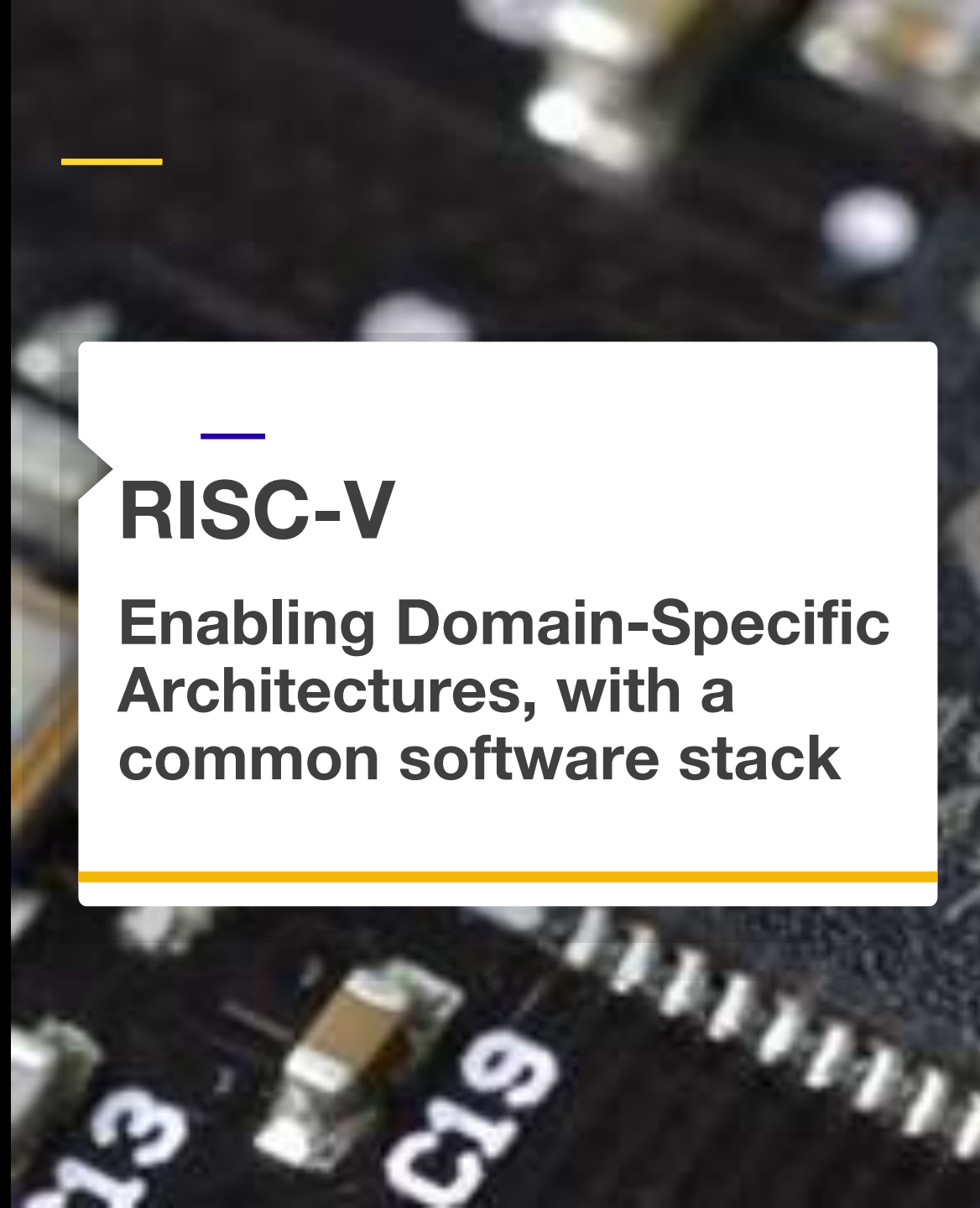
Time for a **Paradigm Shift**

01 Customization is only way to get performance

02 One-Chip-Fits-All no longer applies

03 Innovation desperately needed to meet needs of new applications running on billions of devices

Simple, modern, modular ISA	Scales from microcontrollers to supercomputers
	Easily extensible
Free and open architecture	Freedom to choose
	Software ecosystem fostered by many
	Allows differentiation, specialization, optimization



RISC-V

Enabling Domain-Specific Architectures, with a common software stack

The SiFive Solution

SiFive

SiFive RISC-V Core IP Product Series

E Cores | S Cores

Industry leading 32-bit and 64-bit Embedded Cores

7 Series High Performance Embedded	Storage Networking Automotive	S76 S76-MC E76 E76-MC
3/5 Series Small, Efficient, Performance	Industrial Modems Storage	S51 S54 E31 E34
2 Series SiFive's Most Efficient Series	Microcontrollers IoT Wearables	E21 E24 E20 S21

U Cores

High performance 64-bit Application Cores

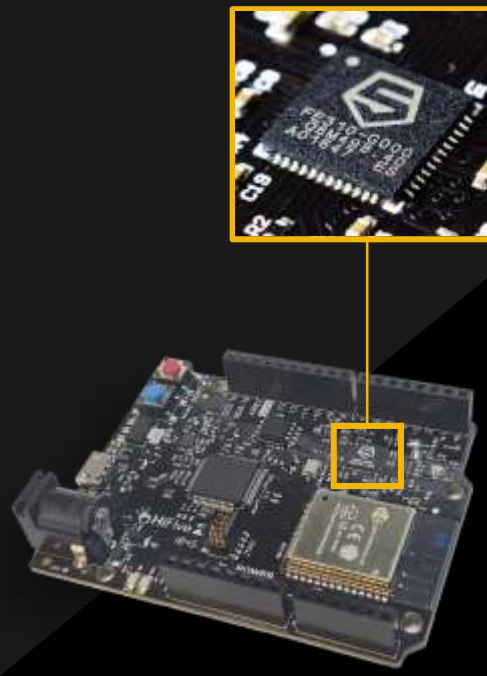
7 Series Optimized High-Performance	SBC Networking Consumer	U74 U74-MC
5 Series Multi-Core RISC-V Linux	Low Cost Linux Industrial Gateways	U54-MC U54

>125 Design wins

RISC-V Development Happens on HiFive Development Boards

HiFive1 RevB

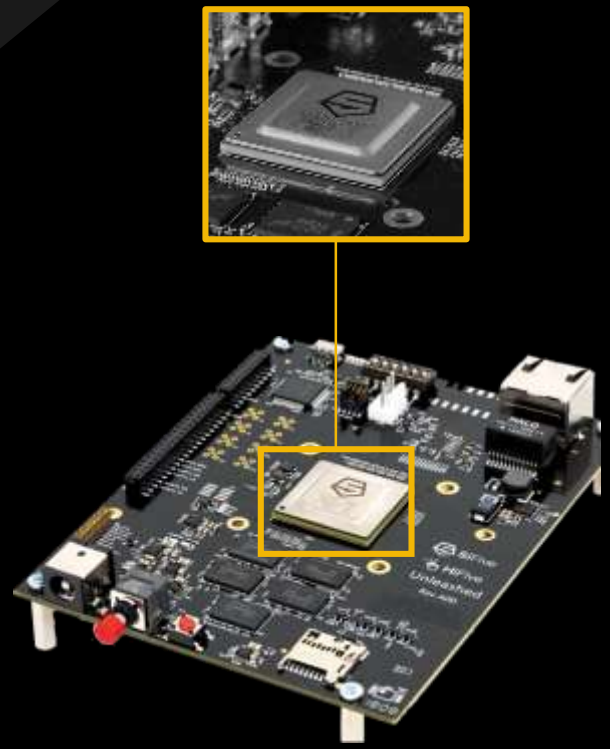
FE310 (E31) Dev Kit



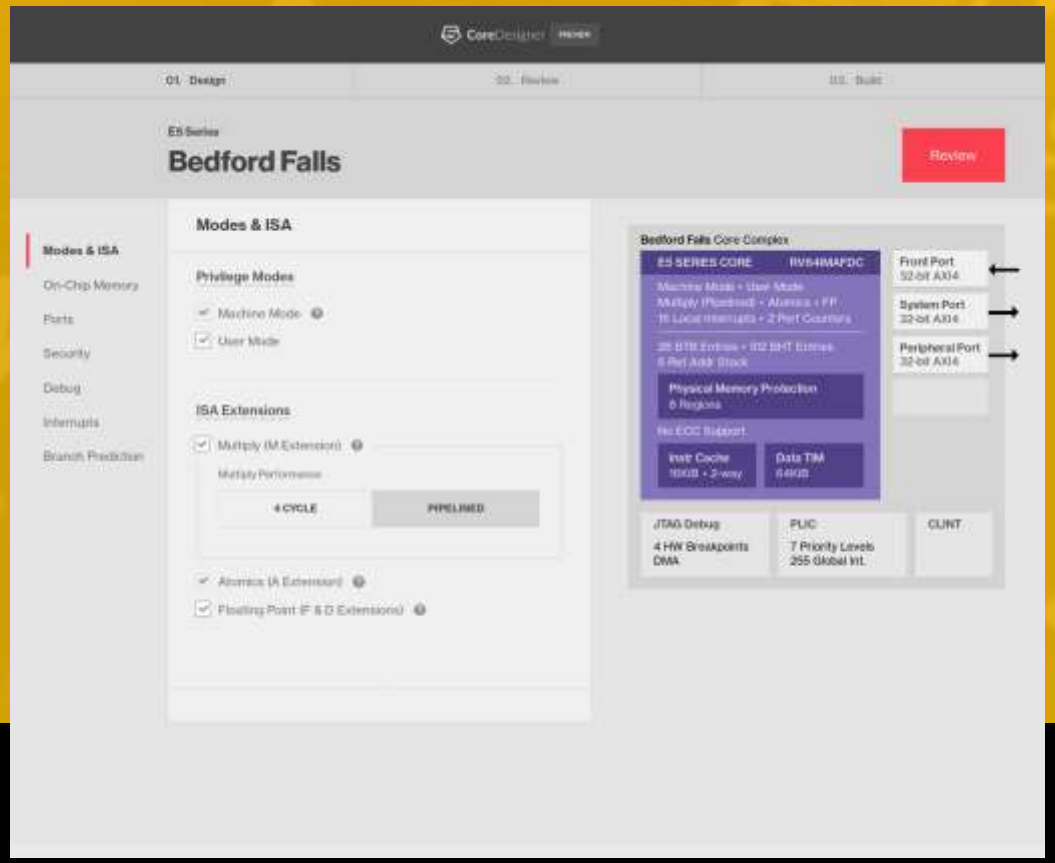
HiFive Unleashed

+ Microsemi Expansion Board

World's First RISC-V Linux Dev Kit



Cloud Delivery: SiFive Core Designer



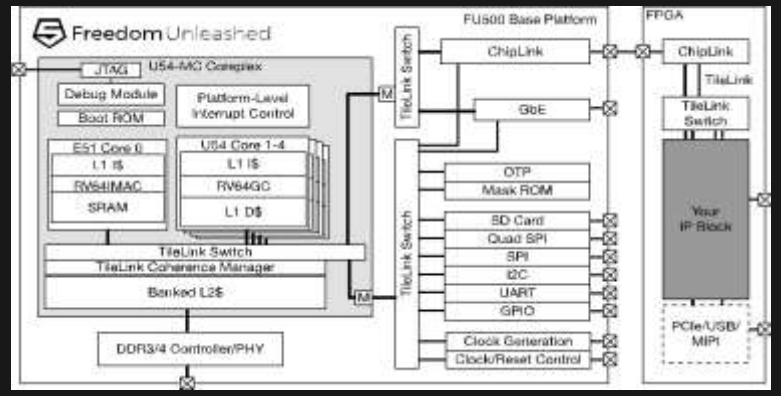
All RISC-V core products are delivered via web-based GUI SiFive **Core Designer**

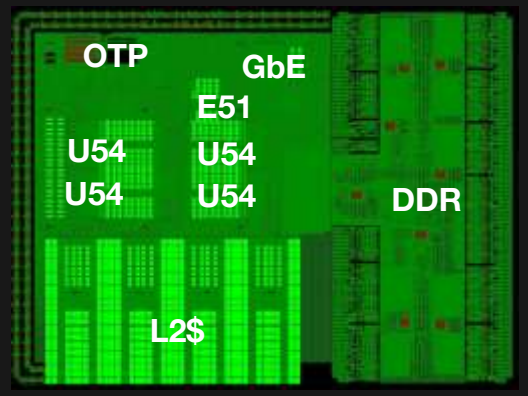
Customers can choose preset Standard Core options or create and save their own configurations

Release Candidates are generated with a single click and available in 24 hours after verification

Our approach has produced many world firsts

World's First Cloud Tape-Out with Microsoft





1.5+ GHz U54-MC SiFive CPU
1x E51: 16KB L1I$, 8KB DTIM with ECC support
4x U54: 32KB L1I$, 32KB L1D$ with ECC support
ChipLink
Serialized Chip-to-Chip
Coherent TileLink Interconnect
DDR3/4, GbE, Peripherals

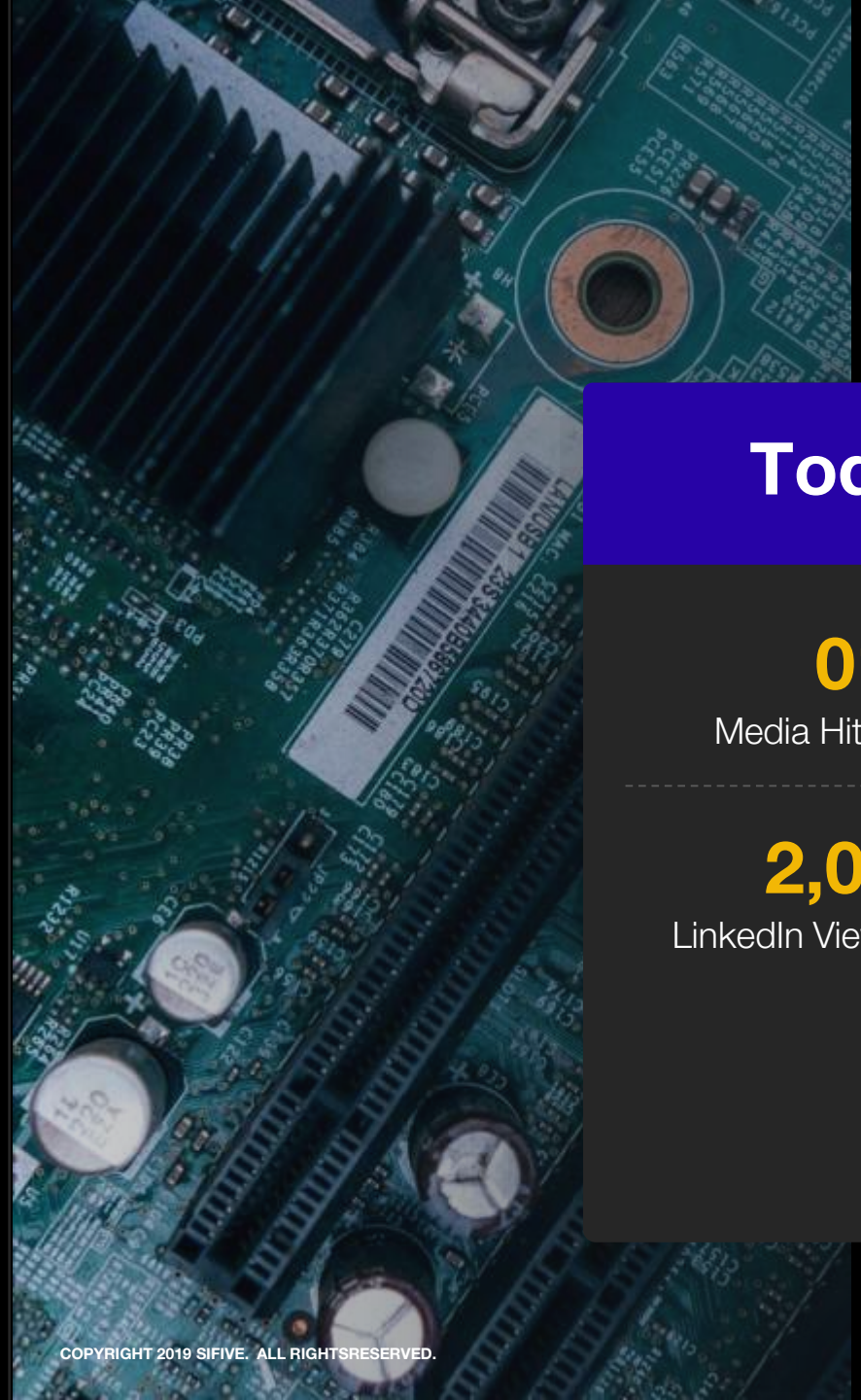
World's First RISC-V SSD Controller

SiFive's RISC-V Core IP was **1/3 the power** and **1/3 the area** of competing solutions, and gave FADU the flexibility we needed in optimizing our architecture to achieve these groundbreaking products."

– Jihyo Lee, FADU CEO

Media News and Awards

SiFive



SiFive Momentum Unprecedented in the Semiconductor Industry

Today	This Week	This Year
01 Media Hit Per Day	**01** Press Release Per Week	**75** Cities
2,000 LinkedIn Views Per Day	**02** Global Events Per Week	**350** Talks
	200 Event Registrations	**6,000,000** Video Views

SiFive
Recognized as a Leader

"More power-efficient than ARM's competing processor designs"

"A tenth of the price in a fifth of the time"

"RISC-V on the Verge of Broad Adoption"

"RISC-V Climbs Software Mountain"

"Is the data center next?"

"SiFive Sees Big Year for RISC-V"

"Anyone with a web interface will be able to design chips and solve problems"

GSA 2018 Award: SiFive Recognized as Most Respected Private Semiconductor Company

Thank You!

SiFive

SiFive

Embedded Intelligence from Edge to Cloud

U Cores

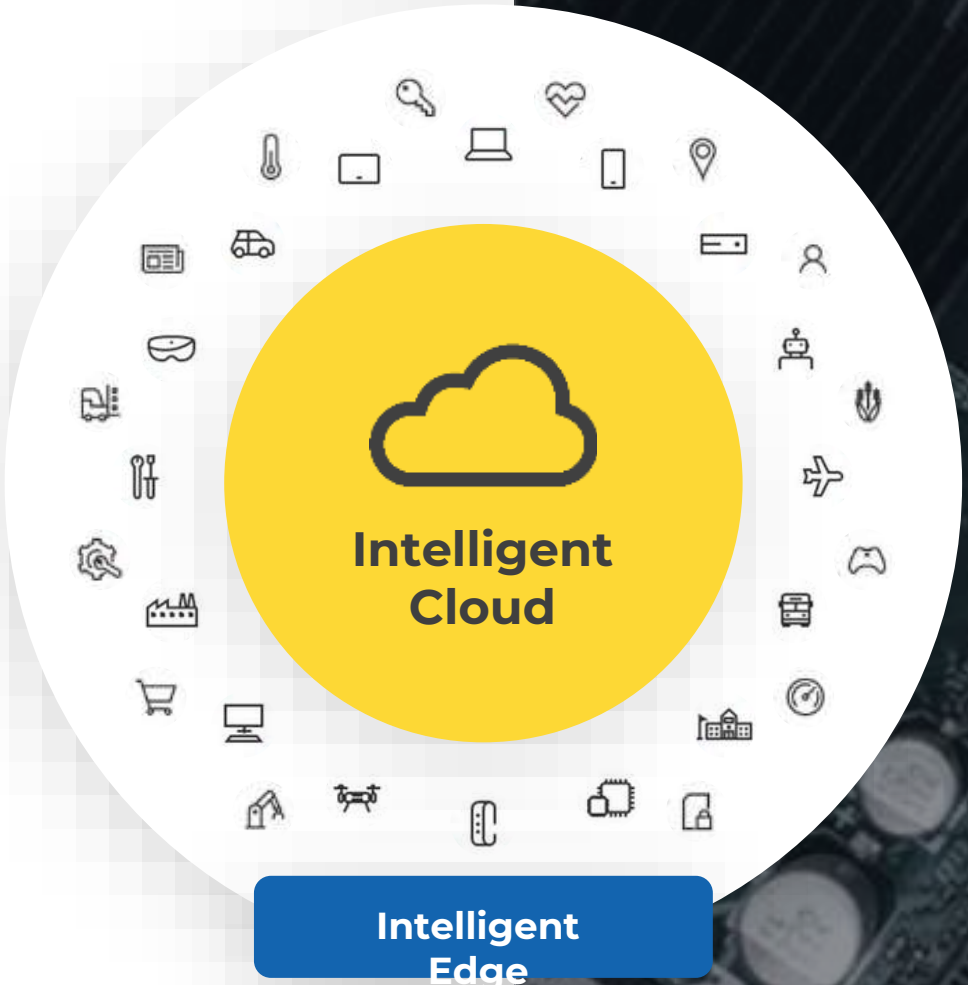
64-bit Application Processors

S Cores

64-bit Embedded Processors

E Cores

32-bit Embedded Processors



Embedding Intelligence from the Edge to the Cloud

SiFive Core IP
Embedding Intelligence Everywhere

Consumer

AR/VR/Gaming devices

Smart Home

Imaging/Wearables

Storage/Networking/5G

SSD, SAN, NAS

Base Stations, Small cells, APs

Switches, Smart NICs, Offload cards

ML/Edge

Sensor Hubs, Gateways

Autonomous machines

IoT devices

SiFive

AR/VR/Sensor Fusion

Low Latency peripheral access and coherent accelerator port

Combine with SiFive 2, 3 or 5 series for designs with tight power constraints

Coherent in-cluster combination of application processors with real time processors

Workload specific customizations (AR/VR/MR/CV)

Simple caching hierarchy for ease of application optimization

Mixed precision arithmetic for accelerating machine learning compute

Storage

Coherent in-cluster combination of application processors and real-time processors

Deterministic mode for **FAST DATA** applications with hard real-time constraints

Configurable memory maps and coherent accelerator ports for tightly coupling storage specific accelerators

Tightly integrated memories and Cache lock capability for critical real time workloads

Optional FPU for applications which don’t need floating point capability

Storage, ML, Cryptography specific **custom instructions**

64-bit real-time addressability for **BIG DATA** applications

5G/Networking

Complex arithmetic capability for accelerating baseband functions

In-cluster coherence of application and real-time processor enables 5G latency (<1ms) requirements

High bandwidth accelerator ports for enabling intelligent offload processing

Hard real-time capabilities for scheduling baseband protocol layers

Configurable memory maps for optimizing QoS

High throughput processing for next gen 5G stacks

Tightly Integrated Memories and Cache lock capability for critical real time workloads

SiFive Core IP – >>125 Design Wins!

Efficient Performance

Scalability

Compelling Feature Set

→

Embedding intelligence for a world of a **Trillion Connected Devices**