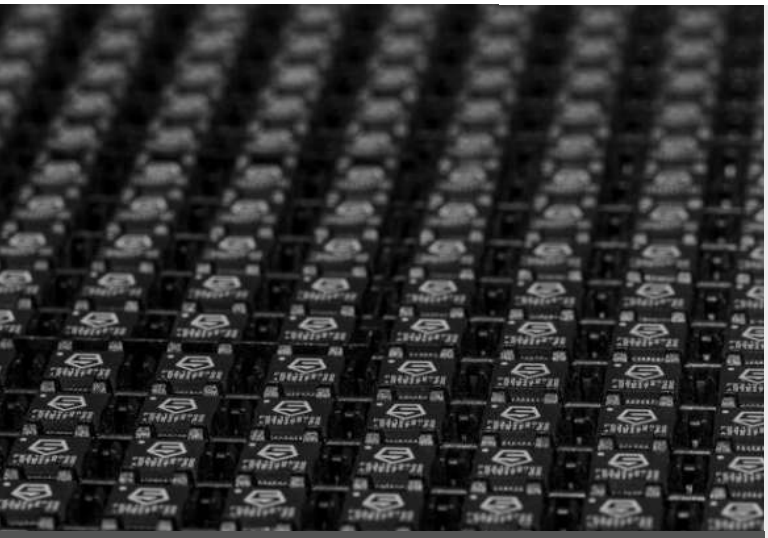
SiFive

SiFive Company Profile



SiFive China

- Best in class in RISC-V based solution with local customer support
- Leader in RISC-V eco system development to support China semiconductor industry, growing with open-source community
- Pineer in Cloud based SaaS service for custom ASICs

Leader in RISC-V Processor IP

- Leading provider of commercial RISC-V processor IP
- Comprehensive roadmap of RISC-V processor IP: from micro-controllers, embedded, to high-performance multi-core Linux capable processors
- Very easy to customize

Leader in taking Semiconductor to the Cloud

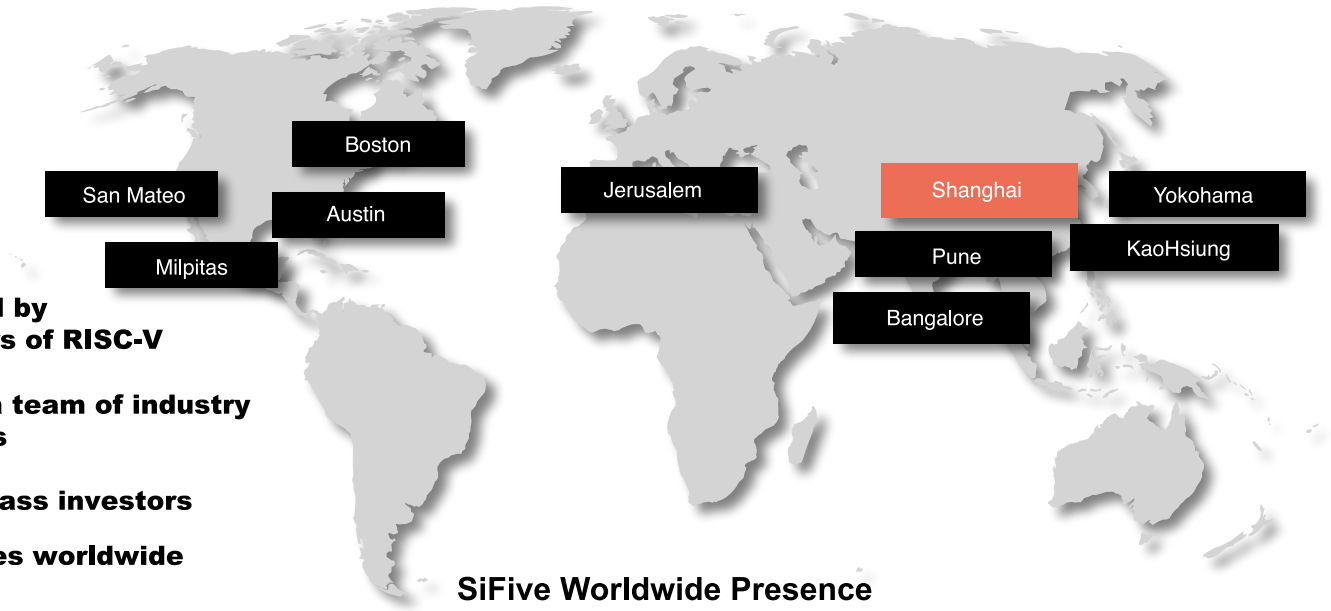
- Leverages software, high-level design, and automation
- Dramatically reduces cost and increase innovation
- Builds custom CPU IP and ASICs on the Cloud

Founded by inventors of RISC-V

Led by a team of industry veterans

World class investors

10 offices worldwide



SiFive Worldwide Presence

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Belief

We believe that by bringing the power of open-source and agile hardware design to the semiconductor industry, SiFive reduces the cost to harness the performance and energy-efficiency of custom silicon to the smallest company, inventor, or maker, enabling a whole new range of applications.

Technology

Built off the most advanced RISC-V Cores in the world, we leverage the power of open source to deliver the industry's first open-source chip platform.

Team

The inventors of RISC-V joined forces with seasoned industry veterans, together bringing a new approach to semiconductors along with decades of industry experience, hundreds of tapeouts and millions of chips shipped.

SiFive RISC-V Core IP

Core Series are customizable to meet your requirements

Standard Cores are pre-configured, silicon-proven implementations

E Cores | S Cores

Industry leading 32-bit and 64-bit Embedded Cores

7 Series — High Performance Embedded

Storage | Networking | Automotive

S76 | S76-MC | E76 | E76-MC

3/5 Series — Small, Efficient, Performance

Industrial | Modems | Storage

S51 | S54 | E31 | E34

2 Series — SiFive's Most Efficient Series

Microcontrollers | IoT | Wearables

E20 | E21 | E24

U Cores

High performance 64-bit Application Cores

7 Series — Optimized High-Performance

SBC | Networking | Consumer

U74 | U74-MC

5 Series — Multi-Core RISC-V Linux

Low Cost Linux | Industrial | Gateways

U54 | U54-MC

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E2 Series

Our smallest, lowest power,
32-bit RISC-V embedded cores

The E2 Series is highly-optimized for area and power while still offering class-leading performance. Targeted for microcontroller and embedded devices, the E2 Core can be configured to have an efficient 2-stage pipeline or a higher performance 3-stage pipeline as well as a Core Local Interrupt Controller (CLIC) enabling extremely fast interrupt response. The E2 Series can be fully customized to meet your specific requirements.

SiFive's Smallest, Lowest Power, Core Series

- Clean sheet design from the inventors of RISC-V
- New interrupt controller enabling fast interrupt handling
- Support for Heterogenous MP with other SiFive Cores

E2 Series Configurability

- **Core** – Tune the E2 for higher performance, or lower area
- **Security** – Support for Memory Protection and RISC-V Machine and User Modes
- **Memory Map** – Fully customizable memory map
- **Ports** – Flexibility in the number and types of ports
- And more – Interrupts, Debug and Trace, Memory Protection, Tightly Integrated Memory

E20 and E21 are Standard Cores within the E2 Series

- Standard Cores are benchmarked with published Power, Performance, and Area
- RTL and FPGA evaluations are available

- ***E2 Series core architectural overview***

  - RV32IMAFCV capable core
  - 2-3 stage, optional, Harvard Pipeline

- ***Very small***

- ***Efficient memory accesses***

  - Ability to add multiple outbound Ports
  - Optional Tightly Integrated Memory (TIM)

- ***First RISC-V core with support for the RISC-V Core Local Interrupt Controller (CLIC)***

  - Provides hardware interrupt prioritization and nesting

- ***SiFive Custom Instruction Extension (SCIE)***

  - Easily add support for custom instructions

- ***Drop In Cortex-M0+ and Cortex-M3/M4 replacement***

  - 10% or more performance uplift vs Cortex-M4

E2

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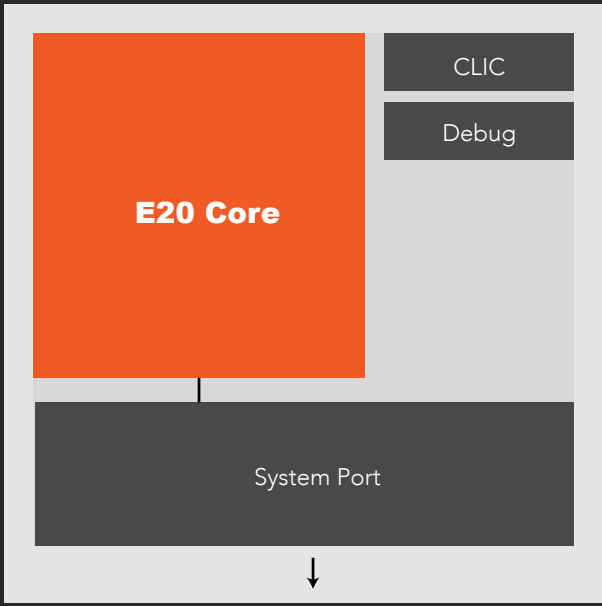
E20

The SiFive E20 Standard Core is an extremely efficient implementation of the E2 Series configured for lowest area and power. The E20 brings the power of the RISC-V software ecosystem to efficiently address traditional 8-bit and 32-bit Microcontroller applications such as IoT, Analog Mixed Signal, and Programmable Finite State Machines.



- ***SiFive's Most Efficient Standard Core***
  - 0.023mm^2 in TSMC 28HPC for entire Core Complex including CLIC, Debug, and System Port
  - 1.1DMIPS/MHz, 2.4 Coremarks/MHz
- ***E20 Standard Core is optimized for Area and Power***
  - Single Core Interface for all Instruction and Data accesses
  - 4 cycle hardware multiply
  - Single System Port Interface
- ***4 Hardware breakpoint/ watchpoints***
- ***Extreme low latency interrupt handling***
  - Execute first instruction of C handler in **6 cycles**
  - Execute entire ISR in **18 cycles**

E20 (AHB-Lite) Post-Route Physical Design

	TSMC 28nm HPC		UMC 55nm LP	
Frequency @ worst setup corner	50 MHz	725 MHz	50 MHz	250 MHz
worst setup corner	ssg_0p81v_m40c_cworst		ss_1p08v_125c_Cmax	
Implementation Details	9t; LVT, SVT,UHVT	12t; LVT, SVT,UHVT	7t; LVT, SVT,UHVT	7t; LVT, SVT,UHVT
Core Complex Area (mm^2)*	0.023	0.046	0.064	0.083
Core Only Area (mm^2)**	0.011	0.029	0.031	0.049
Core Complex Power - Dhrystone (mW) @ worst setup frequency	0.58	18	1.3	8.8
Power Characterization Corner	tt_0p9v_25c_typical		tt_1p2v_25c_Typ	

Note: All area and power numbers do not include RAMs

* Core Complex includes the Core plus CLIC w/32 irq and 2 priority bits, Debug w/ 4 hw breakpoints, internal bus and ports

**Core only includes the core pipeline only

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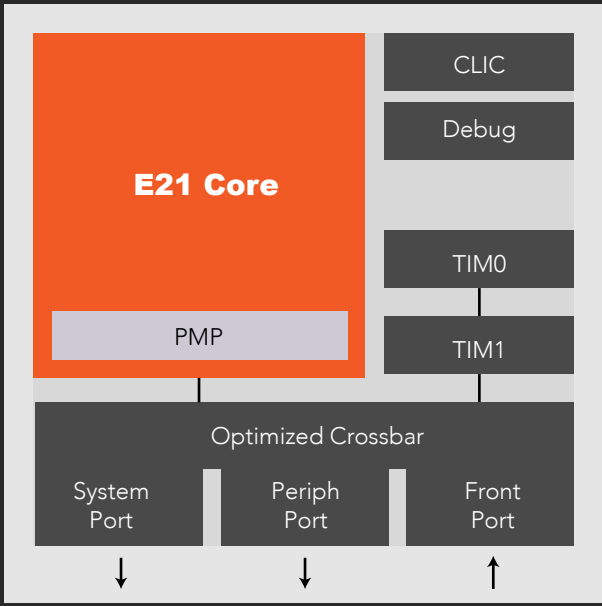
E21

The SiFive E21 Standard Core is a high-performance, full featured embedded processor, designed to address advanced Microcontroller applications such Sensor Fusion, Smart IoT, Wearables, Connected Toys, and more. Separate Instruction and Data Buses, along with 2 banks of Tightly Integrated Memory (TIMs) make the E21 an ideal choice for applications with deterministic or demanding memory requirements.



- ***Full Featured RISC-V MCU***
  - 0.037mm2 in TSMC 28HPC for entire Core Complex without TIM RAMs
  - 1.38 DMIPS/MHz, 3.1 Coremarks/MHz
- ***2 Core Interfaces***
  - Allows for simultaneous instruction and data access
- ***Efficient memory system***
  - Banked TIM for fast local memory
  - Simultaneous Instruction and Data Accesses (Harvard Architecture)
- ***User Mode and Physical Memory Protection (PMP)***
  - 4 Region PMP
- ***4 Hardware breakpoint/ watchpoints***
- ***Extreme low latency interrupt handling***
  - Execute first instruction of C handler in **6 cycles**
  - Execute entire ISR in **18 cycles**

E21 (AHB-Lite) Post-Route Physical Design

	TSMC 28nm HPC		UMC 55nm LP	
Frequency @ worst setup corner	50 MHz	585 MHz	50 MHz	210 MHz
worst setup corner	ssg_0p81v_m40c_cworst		ss_1p08v_125c_Cmax	
Implementation Details	9t; LVT, SVT,UHVT	12t; LVT, SVT,UHVT	7t; LVT, SVT,UHVT	7t; LVT, SVT,UHVT
Core Complex Area (mm^2)*	0.037	0.077	0.1	0.146
Core Only Area (mm^2)**	0.015	0.042	0.043	0.074
Core Complex Power - Dhrystone (mW) @ worst setup frequency	1.3	26	3.1	18
Power Characterization Corner	tt_0p9v_25c_typical		tt_1p2v_25c_Typ	

Note: All area and power numbers do not include RAMs

* Core Complex includes the Core plus CLIC w/127 irq and 4 priority bits, Debug w/ 4 hw breakpoints, 4 Region PMP, TIM Logic, internal bus and ports

**Core only includes the core pipeline only

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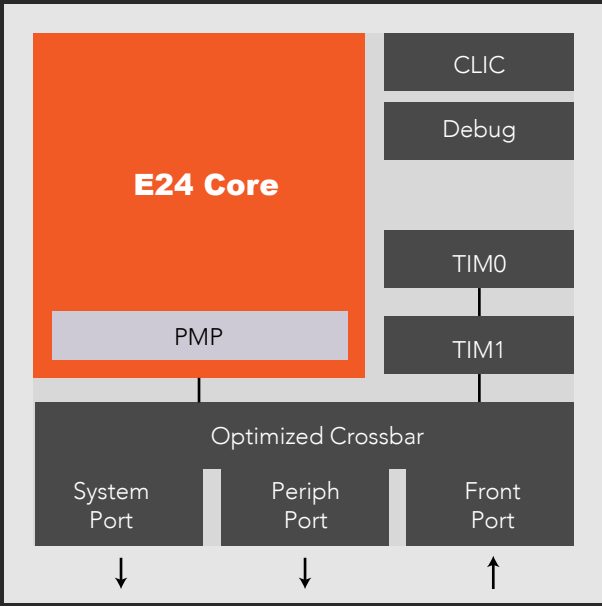
E24

The SiFive E24 Standard Core is a high-performance microcontroller with hardware support for single-precision floating-point capabilities by implementing the RISC-V ISA's F standard extension. The E24's efficiency, coupled with hardware floating-point capabilities, make it exceptional at motor control, sensor fusion, and IoT applications.



Key Features

- ***RISC-V ISA - RV32IMAFC***
  - Includes hardware single-precision floating-point support
- ***Machine and User Mode with 4 Region Physical Memory Protection***
- ***3-stage pipeline with Simultaneous Instruction and Data Access***
- ***2 Banks of Tightly Integrated Memory***
- ***System, Peripheral, and Front Ports***
- ***CLIC interrupt controller with 127 interrupts***
- ***Advanced debug with 4 hardware breakpoints/watchpoints***

E24 (AHB-Lite) Post-Route Physical Design

	TSMC 28nm HPC		UMC 55nm LP	
Frequency @ worst setup corner	50 MHz	565 MHz	50 MHz	214 MHz
worst setup corner	ssg_0p81v_m40c_cworst		ss_1p08v_125c_Cmax	
Implementation Details	9t; LVT, SVT,UHVT	12t; LVT, SVT,UHVT	7t; LVT, SVT,UHVT	7t; LVT, SVT,UHVT
Core Complex Area (mm^2)*	0.049	0.094	0.10	0.15
Core Only Area (mm^2)**	0.028	0.06	0.049	0.078
Core Complex Power - Dhrystone (mW) @ worst setup frequency	1.54	26.4	3.4	19.1
Power Characterization Corner	tt_0p9v_25c_typical		tt_1p2v_25c_Typ	

Note: All area and power numbers do not include RAMs

* Core Complex includes the Core plus CLIC w/127 irq and 4 priority bits, Debug w/ 4 hw breakpoints, 4 Region PMP, TIM Logic, internal bus and ports

**Core only includes the core pipeline only

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E3/S5 Series

High Performance 32bit and
64bit RISC-V MCUs

The E3 Series is highly-integrated and feature-rich. It includes the E31 Core, which is the most widely deployed RISC-V core in the world. E3 embedded cores have a 5-6 stage pipeline, offering a great balance between performance and efficiency.

E3 Series core architectural features

- RV32IMAFCV capable core
- Single Issue, in-order 5-6 stage Harvard Pipeline
  Optional ECC SECDED

Coherent Multi-Core Capable up to 8 cores

- Optional Level 2 Cache Controller

Extremely configurable design to meet different Power, Performance, Area targets

Flexible memory system

- Instruction Cache with ITIM; configurable size
- DTIM or Data Cache; configurable size
- Physical Memory Protection
- Choice of buses: TileLink, APB, AHB, AXI4

Designed for high performance embedded systems:

- Smart IOT
- Wearables
- Embedded Microcontrollers

The S5 Series offers 64-bit RISC-V performance with 32-bit power and area. The S5 core has a 5-6 stage pipeline, offering a great balance between performance and efficiency.

S5 Series core architectural features

- RV64IMAFCV capable core
- Single Issue, in-order 5-6 stage Harvard Pipeline
  Optional ECC SECDED

Coherent Multi-Core Capable up to 8 cores

- Optional Level 2 Cache Controller

Flexible memory system

- Instruction Cache with ITIM; configurable size
- DTIM or Data Cache; configurable size
- Physical Memory Protection
- Choice of buses: TileLink, APB, AHB,
  AXI4 w/ 40bit Physical Address

Ideal for integration into larger 64-bit SoC Systems

- Example uses: “Minion” Core, Boot Processor,
  Security Processor

Great for embedded applications such as:

- SSD Controllers
- Networking Applications

E3 S5

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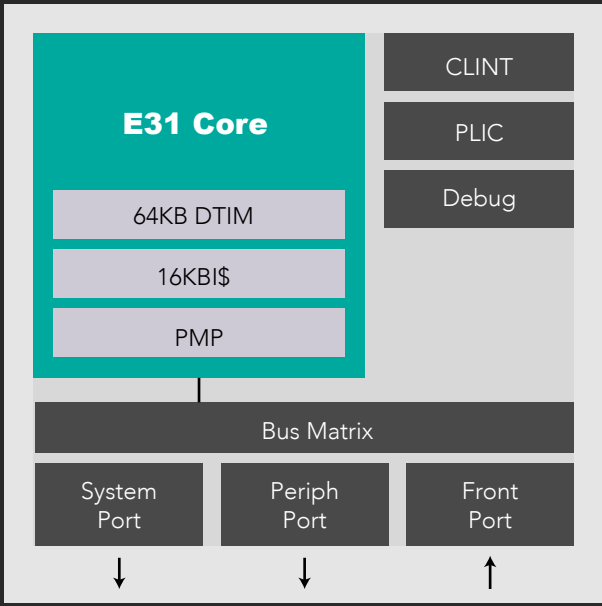
E31

SiFive's E31 Standard Core is the world's most deployed RISC-V core. Co-designed alongside the RISC-V ISA, the E31 takes maximum advantage of the RISC-V ISA, resulting in a power-efficient core that delivers the high performance needed for tomorrow's smart IoT, storage, and industrial applications.



- ***Higher performance***
  - Achieved 320+MHz in TSMC 180G
  - 515.2+ Total DMIPS, 873.6 Total CoreMarks at TSMC180G
  - 300+ MHz in TSMC 180G, 1.5GHz in TSMC 28HPC
  - 1.61 DMIPS/MHz, 3 Coremarks/MHz
- ***Flexible memory architecture***
  - I-Cache can be reconfigured into I-Cache + ITIM
  - DTIM for fast on Core Complex Data Access
  - Off Core Complex memory access through System and Peripheral Ports
- ***Supports local and global interrupts***
  - 127 total interrupts
- ***8 region physical memory protection unit***

E31 (AHB) Synthesis Trials

	TSMC 28nm HPC		UMC 55nm LP	
Frequency (worst)	200 MHz	870 MHz	200 MHz	340 MHz
Implementation Details	9t tt 0p9v 25C	12t tt 0p9v 25C	7t tt 1p2v 25C	7t tt 1p2v 25C
Core Complex Area (mm^2)*	0.082	0.101	0.232	0.267
Core Only Area (mm^2)**	0.053	0.065	0.149	0.183
Core Complex Power (mW)	4.1	26	11.2	24

Note: All area and power numbers do not include RAMs

* CCore only includes the core pipeline, and L1 memory interfaces

** Core Complex includes PLIC w/128/255 irq and 7 priority levels, Debug w/ 4 hw breakpoints, CLINT, internal bus and ports

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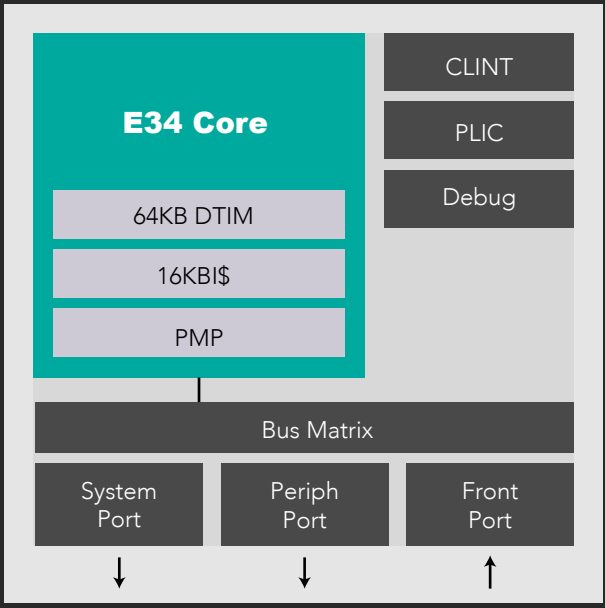
E34

SiFive's E31 Standard Core adds single-precision floating-point to the SiFive E31 Standard Core, the world's most deployed RISC-V core. The E34 enables advanced applications which require hardware floating-point capabilities such as signal processing and motor control.



- ***Fully compliant with the RISC-V ISA specification***

- ***RV32IMAFC Support***
  - RV32I – 32-bit RISC-V with 32 integer registers
  - Integer Multiplication and Division (M) support
  - Atomic (A) extension for high-performance, portable software
  - Floating-Point (F) extension for hardware floating-point instructions
  - Compressed (C) extension for better code density
- ***Machine and User Mode Support***
- ***In-order, 5-6 stage variable pipeline***
- ***Advanced Memory Subsystem***
  - 16KB, 2-way Instruction Cache
  - Instruction Tightly Integrated Memory (ITIM) option
  - Up to 64KB Data Tightly Integrated Memory (DTIM) support
- ***Efficient and Flexible Interrupts***
  - Local interrupts w/ vectored addresses — up to 16
  - Platform Level Interrupt Controller (PLIC) — 127 interrupts w/ 7 priority levels
  - RISC-V Core Local Interruptor (CLINT) — 1 timer, 1 SW
- ***8-Region Physical Memory Protection(PMP)***
- ***High performance TileLink Interface***
- ***1.61 DMIPS/MHz; 3.01 CoreMark/MHz***

E34 (AHB) Post-Route Physical Design

	TSMC 28nm HPC		UMC 55nm LP	
Frequency @ worst setup corner	200 MHz	870 MHz	200 MHz	340 MHz
worst setup corner	ssg_0p81v_m40c_cworst		ss_1p08v_125c_Cmax	
Implementation Details	9t; LVT, SVT,UHVT	12t; LVT, SVT,UHVT	7t; LVT, SVT,UHVT	7t; LVT, SVT,UHVT
Core Complex Area (mm^2)*	0.082	0126	0.23	0.293
Core Only Area (mm^2)**	0.055	0.089	0.15	0.21
Core Complex Power - Dhrystone (mW) @ worst setup frequency	4.8	34.7	12.3	33.8
Power Characterization Corner	tt_0p9v_25c_typical		tt_1p2v_25c_Typ	

Note: All area and power numbers do not include RAMs

* Core Complex includes the Core plus PLIC w/128 irq and 7 priority levels, Debug w/ 4 hw breakpoints, CLINT, internal bus and ports

**Core only includes the core pipeline, and L1 memory interfaces

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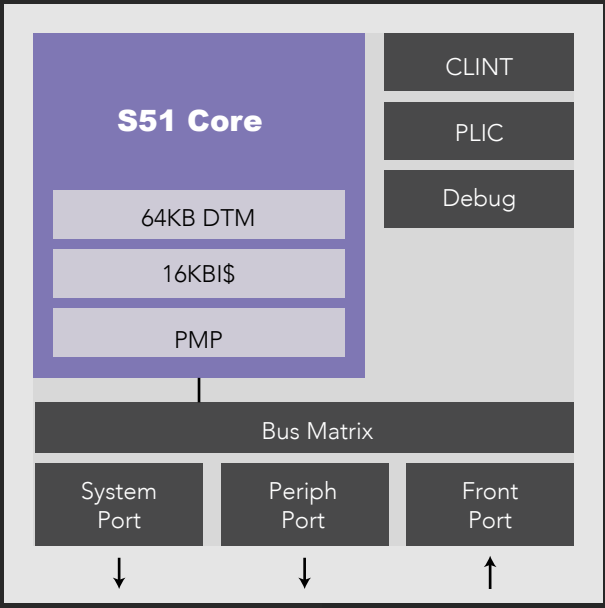
S51

SiFive's S51 Standard Core is a 64-bit embedded processor, fully compliant with the RISC-V ISA. A small-footprint, low-power design makes the S51 ideal for devices that require a tiny system controller in a larger 64-bit SoC. The S51 can also be used as a standalone controller for networking, storage, or other high-performance embedded applications



- ***Better integer performance than 32-bit or smaller architectures***
  - 300+ MHz in TSMC 180G
  - 1.8 DMIPS/MHz, 3 Coremarks/MHz
- ***Supports the RISC-V C Extension***
  - Smaller code size than competing 64-bit architectures
- ***Extended memory map***
  - Support for 40 physical address bits
- ***Supports local and global interrupts***
  - 255 total interrupts

S51 (AHB) Synthesis Trials

	TSMC 28nm HPC		UMC 55nm LP	
Frequency (worst)	200 MHz	870 MHz	200 MHz	340 MHz
Implementation Details	9t tt 0p9v 25C	12t tt 0p9v 25C	7t tt 1p2v 25C	7t tt 1p2v 25C
Core Complex Area (mm^2)*	0.142	0.163	0.404	0.45
Core Only Area (mm^2)**	0.082	0.09	0.233	0.28
Core Complex Power (mW)	5.3	36	15	32

Note: All area and power numbers do not include RAMs

* Core Complex includes the Core plus PLIC w/255 irq and 7 priority levels, Debug w/ 4 hw breakpoints, CLINT, internal bus and ports

**Core only includes the core pipeline, and L1 memory interfaces

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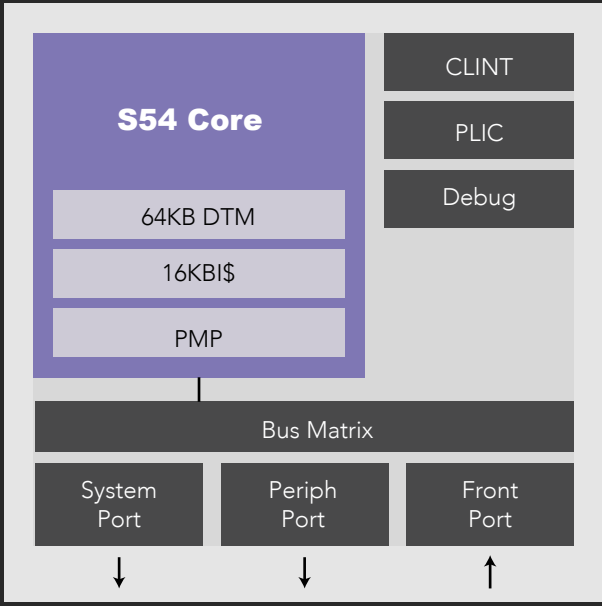
S54

SiFive's S54 Standard Core is a 64-bit embedded processor that is fully-compliant with the RISC-V ISA. It adds support for the F and D standard extensions, which provide the S54 with double-precision floating-point capabilities. The S54 is ideal for demanding applications such as avionics, signal processing, and industrial automation.



- ***Fully compliant with the RISC-V ISA specification***
- ***RV64IMAFC Support***
  - RV64I – 64-bit RISC-V with 32 integer registers
  - Integer Multiplication and Division (M) support
  - Atomic (A) extension for high-performance, portable software
  - F and D extension for hardware double-precision floating-point
  - Compressed (C) extension for better code density
- ***Machine and User Mode Support***
- ***In-order, 5-6 stage variable pipeline***
- ***Advanced Memory Subsystem***
  - 16KB, 2-way Instruction Cache
  - Instruction Tightly Integrated Memory (ITIM) option
  - Up to 64KB Data Tightly Integrated Memory (DTIM) support
- ***Support for up to 40 physical address bits***
- ***Efficient and Flexible Interrupts***
  - Local interrupts w/ vectored addresses — up to 16
  - Platform Level Interrupt Controller (PLIC) — 255 interrupts w/ 7 priority levels
  - RISC-V Core Local Interruptor (CLINT) — 1 timer, 1 SW
- ***8-Region Physical Memory Protection(PMP)***
- ***High performance TileLink Interface***
- ***1.7 DMIPS/MHz; 3.01 CoreMark/MHz***

S54 (AXI) Post-Route Physical Design

	TSMC 28nm HPC		UMC 55nm LP	
Frequency @ worst setup corner	200 MHz	870 MHz	200 MHz	340 MHz
worst setup corner	ssg_0p81v_m40c_cworst		ss_1p08v_125c_Cmax	
Implementation Details	9t; LVT, SVT,UHVT	12t; LVT, SVT,UHVT	7t; LVT, SVT,UHVT	7t; LVT, SVT,UHVT
Core Complex Area (mm^2)*	0.126	0.19	0.36	0.44
Core Only Area (mm^2)**	0.063	0.1	0.177	0.24
Core Complex Power - Dhrystone (mW) @ worst setup frequency	6.8	41.6	10.9	30.8
Power Characterization Corner	tt_0p9v_25c_typical		tt_1p2v_25c_Typ	

Note: All area and power numbers do not include RAMs

* Core Complex includes the Core plus PLIC w/255 irq and 7 priority levels, Debug w/ 4 hw breakpoints, CLINT, internal bus and ports

**Core only includes the core pipeline, and L1 memory interfaces

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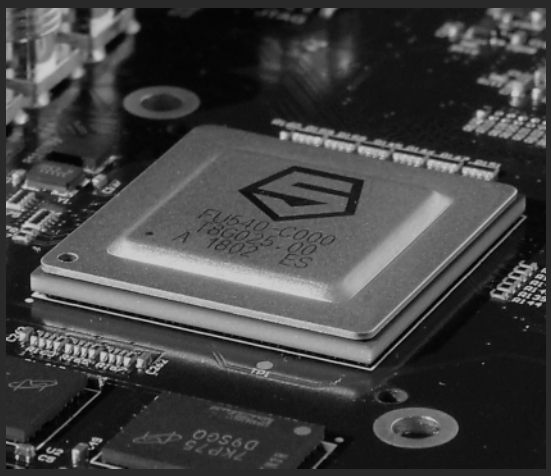
U5 Series

RISC-V Linux-capable application processors with high performance & maximum efficiency

The U5 Series is the world's 1st RISC-V Linux capable core. The U5 Series enables 64-bit RISC-V applications with the efficient U5 Core which has a 5-6 stage pipeline and support for Virtual Memory. Its capable core with high performance and optimized for maximum efficiency.



- ***U5-MC allows for instantiation of up to 9 U5 and/or E5 cores as well as a configurable Level 2 Cache***
- ***U5 Core Architectural Features***
  - RV64GCV capable core with Sv39 Virtual Memory Support
  - Single Issue, in-order 5-6 stage Harvard Pipeline
  - Optional SECDED ECC support on Level 1 and Level 2 memories
- ***Flexible memory system allows for application specific resource partitioning***
  - L2 can be split into part cache, part fast addressable RAM
- ***Configurable E5X minion cores can provide a variety uses***
  - System boot and monitor, Sensor Hub/Fusion, Security Co-Processor
- ***Broad market applications***
  - General purpose embedded, industrial, IoT, high-performance real-time embedded, automotive

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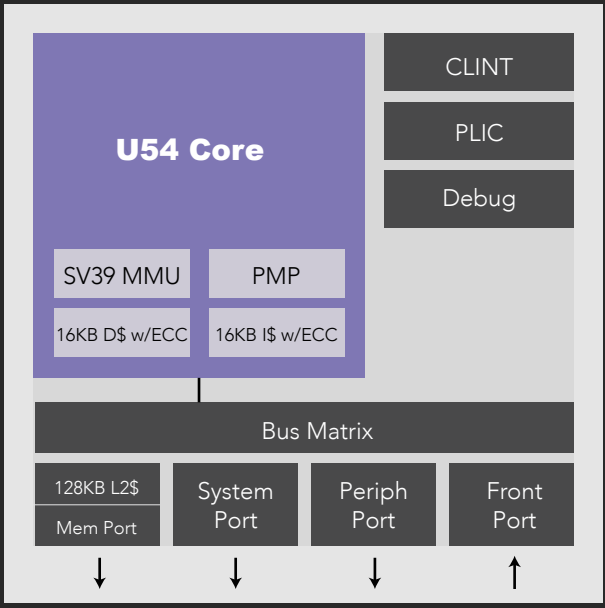
U54

SiFive's U54 Standard Core is a single-core instantiation of the world's first RISC-V application processor, capable of supporting full-featured operating systems such as Linux.

The U54 is ideal for low-cost Linux applications such as IoT nodes and gateways, point-of-sale, and networking.



Key Features

- ***Fully compliant with the RISC-V ISA specification***
- ***RV64GC U54 Application Core***
  - 16KB L1 I-cache with ECC
  - 16KB L1 D-cache with ECC
  - 8 Region Physical Memory Protection
  - 48 Local Interrupts per core
  - Sv39 Virtual Memory support with 38 Physical Address bits
- ***Integrated 128KB L2 Cache with ECC***
- ***Real-time capabilities***
  - 16KB L1 I-cache with ECC
- ***CLINT for multi-core timer and software interrupts***
- ***PLIC with support for up to 128 interrupts with 7 priority levels***
- ***Debug with instruction trace***

	U5 Series
Instruction Set Architecture	RV64GC M + S + U Mode
Compressed Instruction Support	16-bit instructions
Physical Memory Protection	PMP and MMU
Responsiveness	Real-time capable
Interrupt Controller	Integrated
Cores	Up to 8 cores (heterogeneous)

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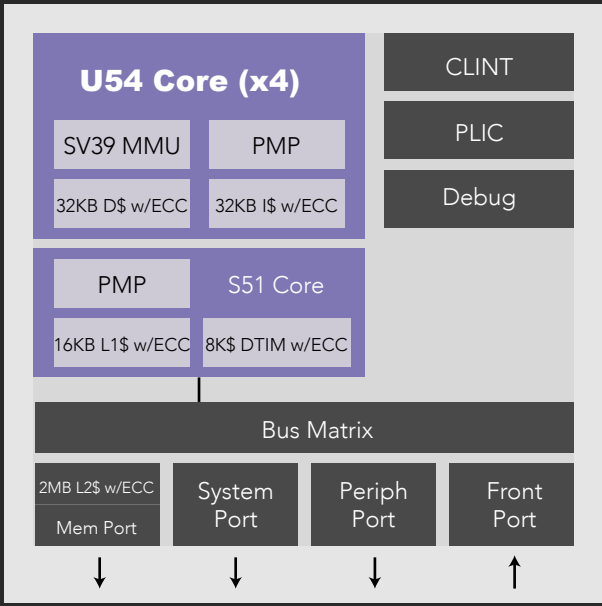
U54-MC

SiFive's U54 Standard Core is the world's first RISC-V application processor, capable of supporting full-featured operating systems such as Linux.

The U54-MC has 4x 64-bit U5 cores and 1x 64-bit S5 core—providing high performance with maximum efficiency. This core is an ideal choice for low-cost Linux applications such as IoT nodes and gateways, storage, and networking.



U54-MC Standard Core IP Power, Performance, and Area

	28nm HPC
U54 Core-Only Area[a]	0.234 mm^2
U54 Core Complex Area[b] (with 32KB I$/32KB D$)	0.538 mm^2
Frequency[c]	Typical: 1.5GHz Worst: 960MHz

[a] Single U54 Core-only data, excludes SRAM; 85% utilization
[b] Core Complex data includes single U54 core, 32KB I-Cache, 32KB D-Cache, PLIC, Debug
[c] 12 track standard cells. Typical: TT Corner @ 0.9V, 25C, Worst: Slow/Slow, 0.81V, -40C

Key Features

- ***Fully compliant with the RISC-V ISA specification***
- ***4x RV64GC U54 Application Cores***
  - 32KB L1 I-cache with ECC
  - 32KB L1 D-cache with ECC
  - 8 Region Physical Memory Protection
  - 48 Local Interrupts per core
  - Sv39 Virtual Memory support with 38 Physical Address bits
- ***1x RV64IMAC S51 Monitor Core***
  - 16KB L1 I-Cache with ECC
  - 8KB DTIM with ECC
  - 8 Region Physical Memory Protection
  - 48 Local Interrupts
- ***Fully Coherent TileLink Bus***
- ***Integrated 2MB L2 Cache with ECC***
- ***Real-time capabilities***
  - Both the L1 Instruction Cache and the L2 Cache can be configured into high speed deterministic SRAMs
- ***CLINT for multi-core timer and software interrupts***
- ***PLIC with support for up to 511 interrupts with 7 priority levels***
- ***Debug with instruction trace***
- ***U54 Performance***
  - 1.7 DMIPS/MHz
  - 2.75 CoreMark/MHz

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SiFive Core IP 7 Series

Announcing the highest performance commercial RISC-V processor IP

E7 Series

Ultra-High Performance 32-bit Embedded Processors

- Unprecedented Performance/Watt/mm2
- Scalable Multi-Core with Coherency
- Determinism for Hard Real-Time
- Fast, Deterministic, Interrupt Response
- Fast IO Access
- Tightly Coupled Accelerators

S7 Series

Ultra-High Performance 64-bit Embedded Processors

- Unprecedented Performance/Watt/mm2
- Scalable Multi-Core with Coherency
- Determinism for Hard Real-Time
- Fast, Deterministic, Interrupt Response
- Fast IO Access
- Tightly Coupled Accelerators

U7 Series

Ultra-High Performance 64-bit Embedded Processors

- Unprecedented Performance/Watt/mm2
- Scalable Multi-Core with Coherency
- Determinism for Hard Real-Time
- Fast, Deterministic, Interrupt Response

Efficient Performance

***~60% improvement** in CoreMarks/MHz**

***~40% improvement** in DMIPS/MHz**

***~10% improvement** in Fmax**

Scalability

***8+1 coherent CPUs** in a cluster*

512 coherent on-chip CPUs** via **TileLink

2048 multi-socket coherent CPUs** via **ChipLink

Compelling Feature Set

***In-cluster heterogeneous compute** for Application + Real-time processors*

***64-bit architectures** across portfolio*

Innovative L1 Memory microarchitecture

** Compared to SiFive Core IP 5 Series*

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E7/U7/S7 Series

Our highest-performance 32-bit/64-bit RISC-V embedded cores

The E7 Series offers a 32-bit embedded processor targeting applications that require high performance while maintaining energy efficiency. The E7 core has a superscalar 8-stage in-order pipeline.

The U7 Series features SiFive's highest-performance RISC-V Linux-capable application processor. The U7 core has a superscalar 8-stage pipeline with support for virtual memory, enabling the most demanding 64-bit RISC-V applications such as Edge Compute, Big-Data Analytics and 5G Base Stations.

The S7 Series offers a 64-bit embedded processor targeting high-performance, real-time applications that require 64-bit memory addressability. The S7 core has a superscalar 8-stage in-order pipeline.

E7
U7
S7

Key Features

7 core architectural features

- RV32/64GCV capable core
- Dual Issue, in-order 8 stage Harvard Pipeline

Performance and Area

- DMIPS – 2.5 DMIPS/MHz
- Coremark – 4.9 Coremarks/MHz
- Core Area is 30% larger than equivalent 3/5 Series Core

Very Flexible memory system

- Optional I$ and D$
- Optional I and D TCM interfaces
- Optional Fast IO Port (FIO) per core for low latency access to peripheral devices and memories

Functional Safety and Security and Real Time features

- SECDED ECC on all L1 and L2 memories
- User Mode Interrupts for compartmentalization
- Programmatically clear and/or disable dynamic branch prediction for deterministic execution and enhanced security

Multi-Core Capable with Coherency and optional L2

High end embedded applications

- SSD Controllers
- IoT Edge Computing
- Wireless Radios
- Automotive/Industrial

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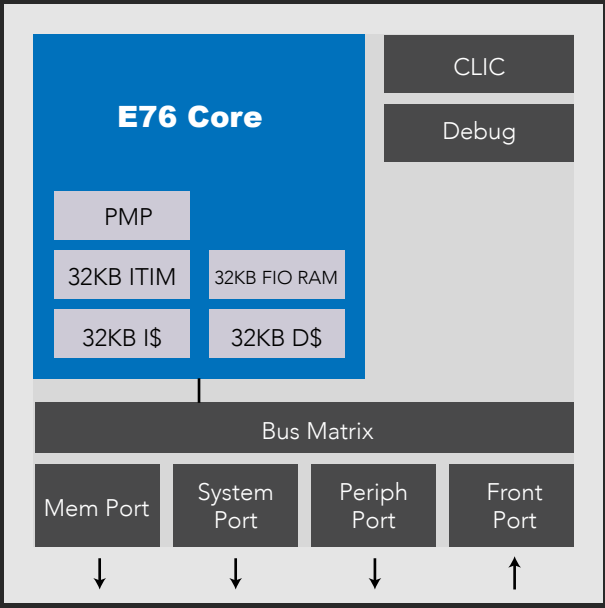
E76

SiFive's E76 Standard Core is a high-performance 32-bit embedded processor which is fully-compliant with the RISC-V ISA. Its advanced memory subsystem enables inclusion of tightly-integrated memory and caches.

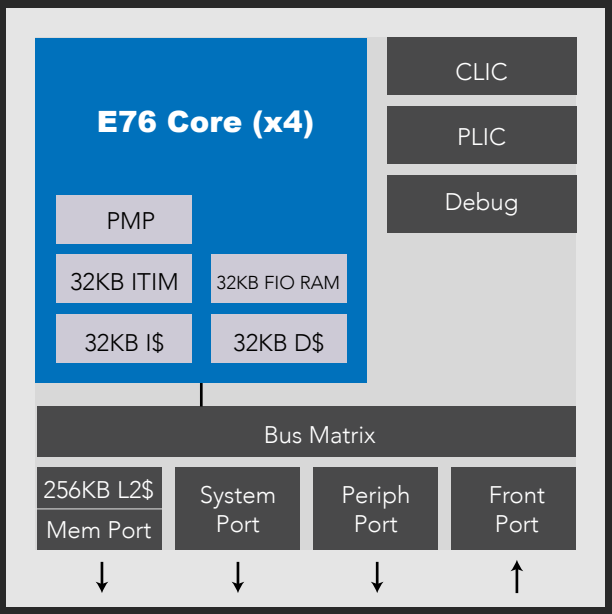
The E76 is ideal for applications which require high performance -- but have power constraints (e.g., Augmented Reality and Virtual Reality , IoT Edge Compute, Biometric Signal Processing, and Industrial Automation).



E76-MC

SiFive's E76-MC Standard Core is a high-performance quad-core 32-bit embedded processor which is fully-compliant with the RISC-V ISA. Its advanced memory subsystem enables inclusion of tightly-integrated memory and caches.

The E76-MC is ideal for applications with high-throughput requirements such as In-storage Compute, Sensor Hubs, Edge-compute Nodes, Biometric Signal Processing, and Autonomous Machines (i.e., Robots, Drones, ADAS systems, etc.)



Key Features

- ***Fully compliant with the RISC-V ISA specification***
- ***E76: RV32IMAFC Cores***
- ***E76-MC: RV32IMAFC E76 Cores (4x)***
- ***Machine and User Mode Support***
- ***In-order, 8-stage pipeline***
- ***High-performance TileLink Interface***
- ***Advanced Memory Subsystem***
  - 32KB Instruction Cache
  - 32KB Instruction Tightly Integrated Memory (ITIM)
  - 32KB Data Cache
  - 32KB FIO RAM

  - E76-MC: 256MB L2 Cache
- ***Benchmark Scores***
  - 2.3 DMIPS/MHz
  - 4.9 CoreMark/MHz

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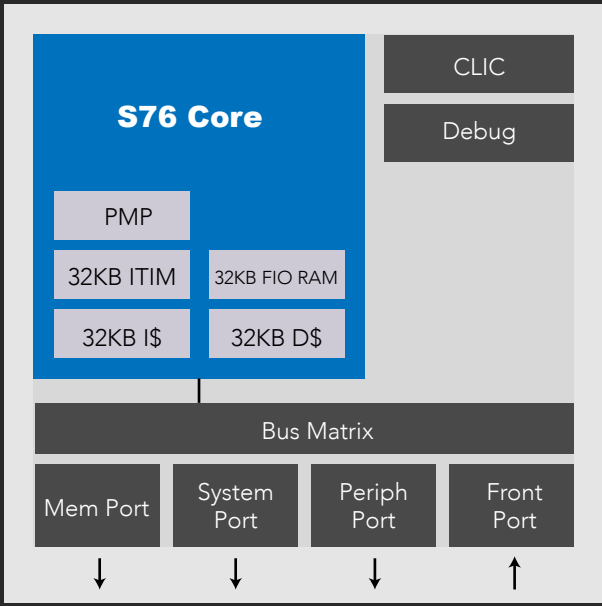
S76

SiFive's S76 Standard Core is a high-performance 64-bit embedded processor which is fully-compliant with the RISC-V ISA.

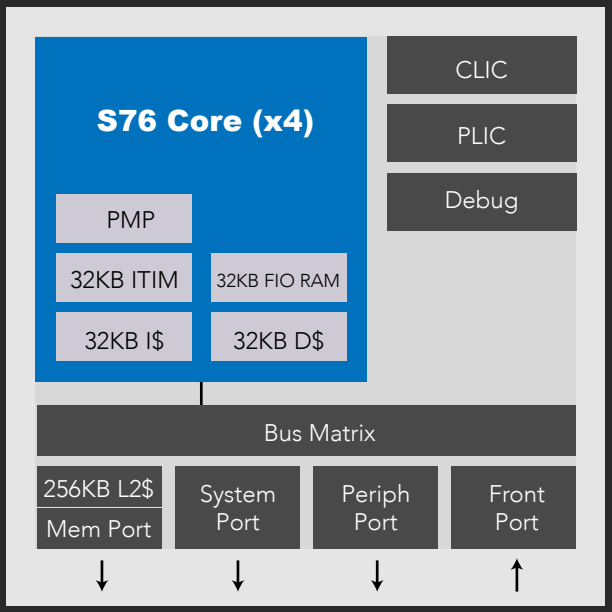
The S76 is ideal for latency-sensitive applications in domains such as storage and networking that require 64-bit memory addressability (e.g. In-storage Compute, Edge Compute, 5G Modems, Object storage etc.)



S76-MC

SiFive's S76-MC Standard Core is a high-performance 64-bit quad-core embedded processor which is fully-compliant with the RISC-V ISA.

The S76-MC is ideal for latency-sensitive applications in domains such as storage and networking that require high-throughput, 64-bit memory addressability, and have real-time constraints (e.g. Enterprise Storage, In-storage Compute, 5G Base Stations, SLAM processing, etc.)



Key Features

- ***Fully compliant with the RISC-V ISA specification***
- ***S76: RV64GC Core***
- ***S76-MC: RV64GC S76 Core(4x)***
- ***Machine and User Mode Support***
- ***In-order, 8-stage pipeline***
- ***High-performance TileLink Interface***
- ***Advanced Memory Subsystem***
  - 32KB Instruction Cache
  - 32KB Instruction Tightly Integrated Memory (ITIM)
  - 32KB Data Cache
  - 32KB FIO RAM
- ***Efficient and flexible interrupts***
- ***Physical Memory Protection (PMP)***
- ***2.5 DMIPS/MHz***
- ***4.9 CoreMark/MHz***

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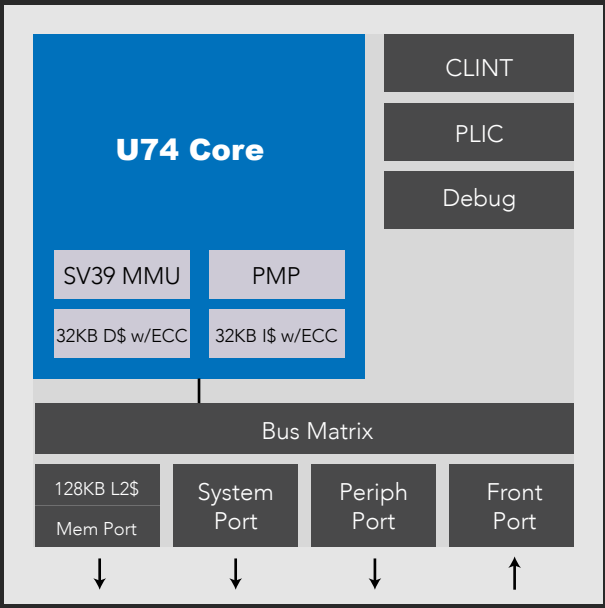
U74

SiFive's U74 Standard Core is a single-core instantiation of the world's highest performance RISC-V application processor, capable of supporting full-featured operating systems such as Linux.

The U74 is ideal for applications requiring high-throughput, single-thread performance -- but have power constraints (e.g., AR, VR, sensor hubs, IVI systems, IP cameras, digital cameras, gaming devices, etc.)



Key Features

- ***Fully compliant with the RISC-V ISA specification***
- ***RV64GC U74 Application Core***
  - 32KB L1 I-cache with ECC
  - 32KB L1 D-cache with ECC
  - 8 Region Physical Memory Protection
  - 128 Global Interrupts per core
  - Sv39 Virtual Memory support with 38 Physical Address bits
- ***Integrated 128KB L2 Cache with ECC***
- ***CLIC for timer and software interrupts***
- ***PLIC with support for up to 128 interrupts with 7 priority levels***
- ***Benchmark Scores***
  - 2.5 DMIPS/MHz
  - 4.9 CoreMark/MHz

U74 (AXI) Post-Route Physical Design

	TSMC 28nm HPC
Frequency @ worst setup corner	887 MHz
worst setup corner	ssg_0p81v_m40c_cworst
Implementation Details	12t; LVT, SVT,UHVT
Core Complex Area (mm^2)*	0.577
Core Only Area (mm^2)**	0.269
Core Complex Power - Dhrystone (mW) @ worst setup frequency (includes leakage)	106
Power Characterization Corner	func_tt_0p9v_25c_typical

Note: All area and power numbers do not include RAMs

* Core Complex includes the Core plus PLIC w/255 irq and 7 priority levels, Debug w/ 4 hw breakpoints, CLINT, internal bus and ports

**Core only includes the core pipeline, and L1 memory interfaces

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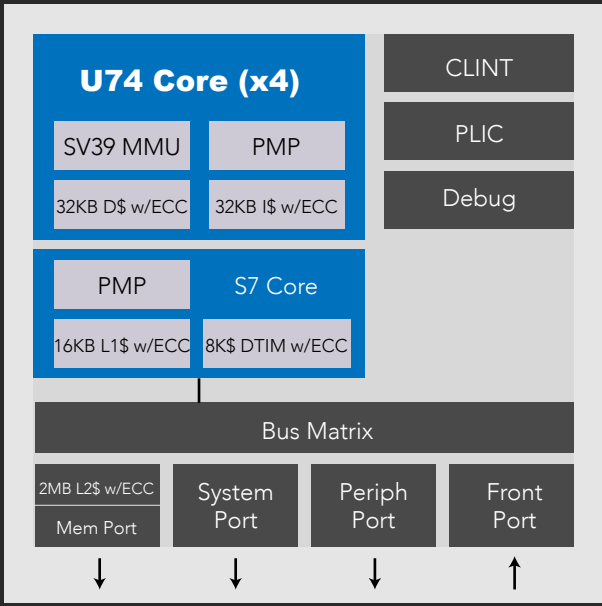
U74-MC

SiFive's U74 Standard Core is the world's highest performance RISC-V application processor, capable of supporting full-featured operating systems such as Linux. The U74-MC has 4x 64-bit U74 cores and 1x 64-bit S7 core -- providing high performance with hard real-time determinism.

This U74-MC is ideal for applications requiring high-throughput performance with real-time guarantees (e.g., Enterprise Storage, Wireless/ Wireline Networking, 5G Baseband Processors, SLAM Processors, Sensor Fusion, etc.)



Key Features

- ***Fully compliant with the RISC-V ISA specification***
- ***4x RV64GC U74 Application Cores***
  - 32KB L1 I-cache with ECC
  - 32KB L1 D-cache with ECC
  - 8 Region Physical Memory Protection
  - Sv39 Virtual Memory support with 38 Physical Address bits
- ***1x RV64IMAC S7 Monitor Core***
  - 16KB L1 I-Cache with ECC
  - 8KB DTIM with ECC
  - 8 Region Physical Memory Protection
- ***U74 and S7 cores are fully-coherent***
- ***Integrated 2MB L2 Cache with ECC***
- ***Real-time capabilities***
  - Both the L1 Instruction Cache and the L2 Cache can be configured into high speed deterministic SRAMs
- ***Debug with instruction trace***
- ***2.5 DMIPS/MHz; 4.9 CoreMark/MHz***

	U74-MC
Instruction Set Architecture	4xRV64GC and 1xRV64IMAC
Compressed Instruction Support	16-bit instructions
Physical Memory Protection	PMP and MMU
Monitor Core	Yes
Interrupt Controller	Optional; pre-Integrated

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Silicon on Cloud

Cloud-based
Customize your own RISC-V core
Unique for your application
Not shared with your competitors

From the Inventors of RISC-V

SiFive - The Largest RISC-V Ecosystem

- SiFive Freedom Studio
  - Eclipse CDT, GNU MCU Eclipse, pre-built GCC, and OpenOCD
  - Built on Open Source technology
- SEGGER
  - SEGGER JLINK for Debug and Production
  - Flash Programming
  - Embedded Studio for RISC-V – IDE,
  - toolchain, debugger
- Lauterbach
  - Lauterbach TRACE32 for silicon bring up and debug
- UltraSoC
  - IP and tooling supporting SiFive instruction trace
- IAR
  - IAR Embedded Workbench with SiFive support in development
- Embedded Operating Systems
  - Express Logic – Thread X
  - FreeRTOS
  - Zephyr OS
  - Micrium - µCOS
  - RIOT
- Rich Operating Systems
  - Debian Linux
  - Fedora Linux
  - SylixOS

SylixOS embedded
LAUTERBACH DEVELOPMENT TOOLS
debian
fedora
Zephyr™
RIOT
SEGGER
FreedomStudio
IAR SYSTEMS
RT-Thread
ultraSoC
expresslogic

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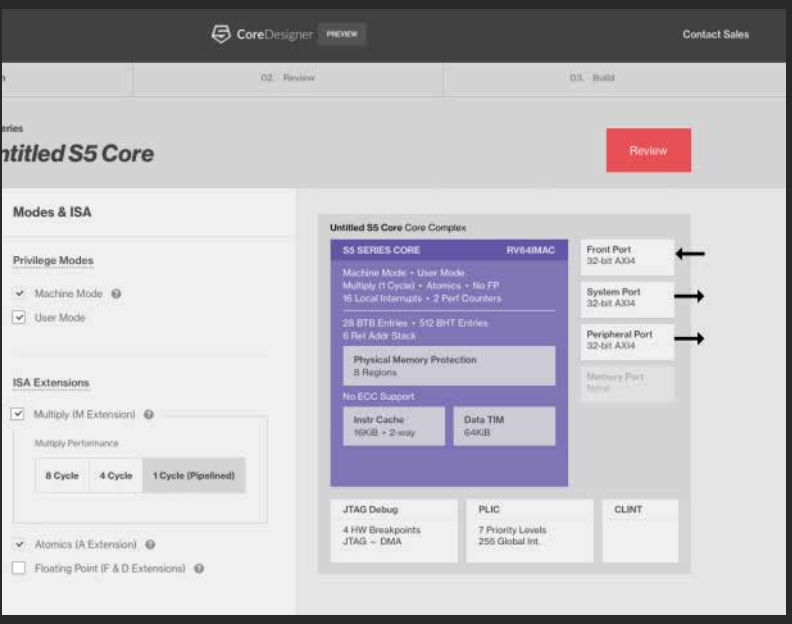
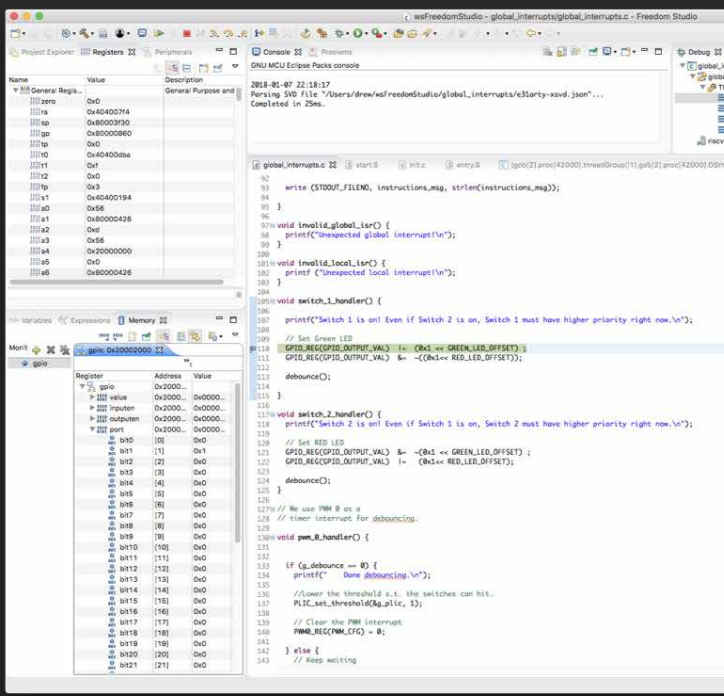
SiFive Core Designer



https://scs.sifive.com/core-designer/

- ***All products are configured and delivered via the SiFive Core Designer Web Portal***
  - Simple, Easy to Use, Web Interface
- ***Preset options to quickly choose Standard Core options***
- ***Configurations can be named and saved for later use***
- ***Power, Performance, Area guidance is given for all parameters***
- ***Release Candidates are generated with click of a button and available from the Developer Dashboard***
  - All Release Candidates are verified via SiFive's verification flow prior to being made available for download

SiFive Freedom Studio



- ***Freedom Studio***
  - Eclipse + CDT + GNU MCU Eclipse
  - Bundled Toolchain and OpenOCD Binaries
  - Example software for SiFive platforms
- ***Peripheral register viewer***
- ***Multicore debug support***
- ***QEMU for simulation of SiFive platforms***
  - Write and validate software before having access to silicon or emulation
- ***Debug probe support***
  - OpenOCD probes such as Olimex
  - SEGGER JLINK
- ***Supports Windows, Mac, Linux***

SiFive

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HiFive1

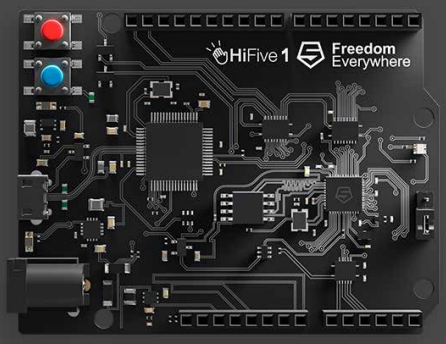
——A RISC-V-based, Open-Source, Arduino-Compatible Development Kit

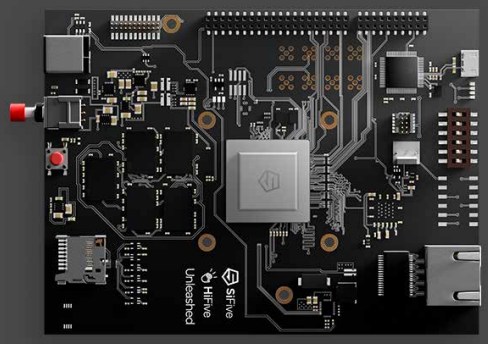
The HiFive1 is an Arduino-Compatible development kit featuring the Freedom E310, the industry's first commercially available RISC-V SoC.

HiFive Unleashed

——The world's first RISC-V-based Linux development board

HiFive Unleashed is the ultimate RISC-V developer board. Featuring the world's first and only Linux-capable, multi-core, RISC-V processor – the Freedom U540 – the HiFive Unleashed ushers in a brand new era for RISC-V.





HiFive1 Features and Specifications

- Microcontroller: SiFive Freedom E310 (FE310)
  - SiFive E31 RISC-V Core
  - Architecture: 32-bit RV32IMAC
  - Speed: 320+ MHz
  - Performance: 1.61 DMIPs/MHz, 2.73 vCoremark/MHz
  - Memory: 16 KB Instruction Cache, 16 KB Data Scratchpad
  - Other Features: Hardware Multiply/Divide, Debug Module, Flexible Clock Generation with on-chip oscillators and PLLs
- Operating Voltage: 3.3 V and 1.8 V
- Input Voltage: 5 V USB or 7-12 VDC Jack
- IO Voltages: Both 3.3 V or 5 V supported
- Digital I/O Pins: 19
- PWM Pins: 9
- SPI Controllers/HW CS Pins: 1/3
- External Interrupt Pins: 19
- External Wakeup Pins: 1
- Flash Memory: 128 Mbit Off-Chip (ISSI SPI Flash)
- Host Interface (microUSB): Program, Debug, and Serial Communication
- Dimensions: 68 mm x 51 mm
- Weight: 22 g

Freedom U540: The First Linux-ready RISC-V Chip

As you expect from SiFive, the Freedom U540 is bleeding-edge RISC-V silicon:

- World's fastest RISC-V Processor
- World's only Linux-capable RISC-V SoC
- 4+1 Multi-Core Coherent Configuration, up to 1.5 GHz
- 4x U54 RV64GC Application Cores with Sv39
- Virtual Memory Support
- 1x E51 RV64IMAC Management Core
- Coherent 2MB L2 Cache
- 64-bit DDR4 with ECC
- 1x Gigabit Ethernet
- Built in 28nm

HiFive Unleashed: The Ultimate RISC-V Developer Board

The HiFive Unleashed Development Board includes:

- SiFive Freedom U540 SoC
- 8GB DDR4 with ECC for serious application development
- Gigabit Ethernet Port
- 32MB Quad SPI Flash from ISSI
- MicroSD Card for removable storage
- FMC Connector for future expansion with add-in cards