



# Enabling Embedded Intelligence

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SiFive China Technology Day

# SiFive Core IP

## Embedding Intelligence Everywhere



### Consumer

AR/VR/Gaming devices

Smart Home

Imaging/Wearables



### Storage/Networking/5G

SSD, SAN, NAS

Base Stations, Small cells, APs

Switches, Smart NICs, Offload cards



### ML/Edge

Sensor Hubs, Gateways

Autonomous machines

IoT devices

# The Evolution of IOT Silicon

## 3 Phases of IOT Evolution



Autonomy (AI)

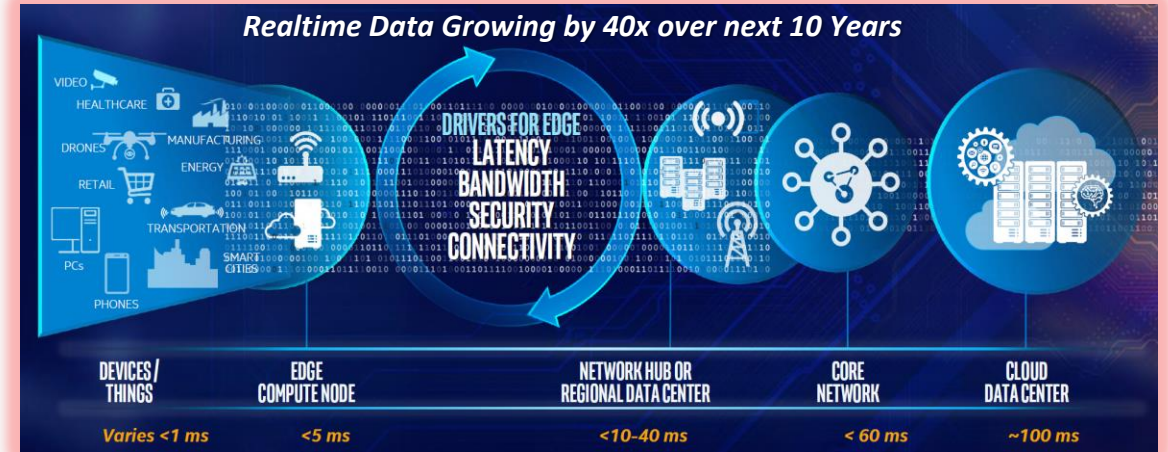


Connectivity

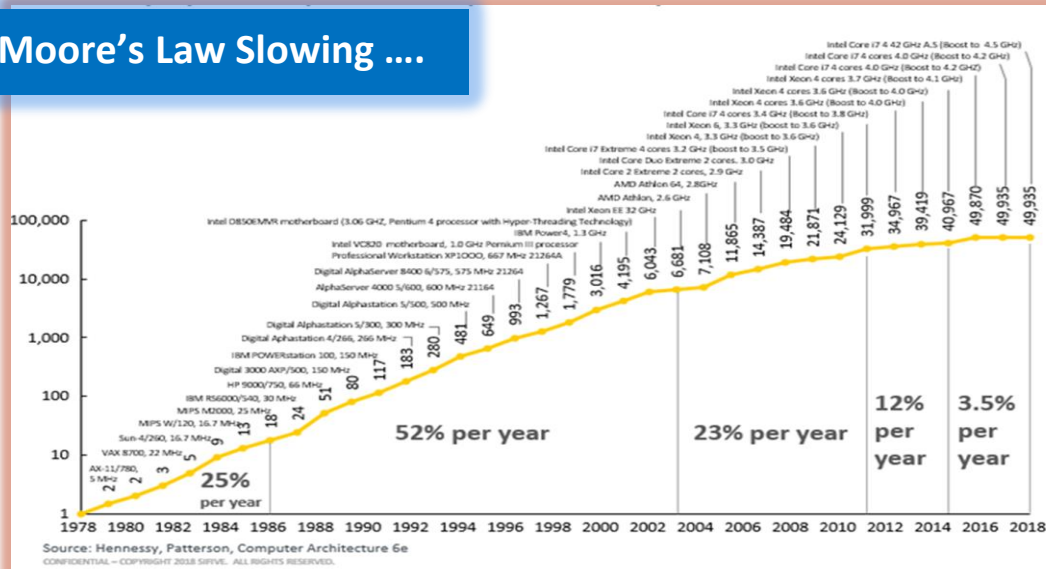


Smart Devices

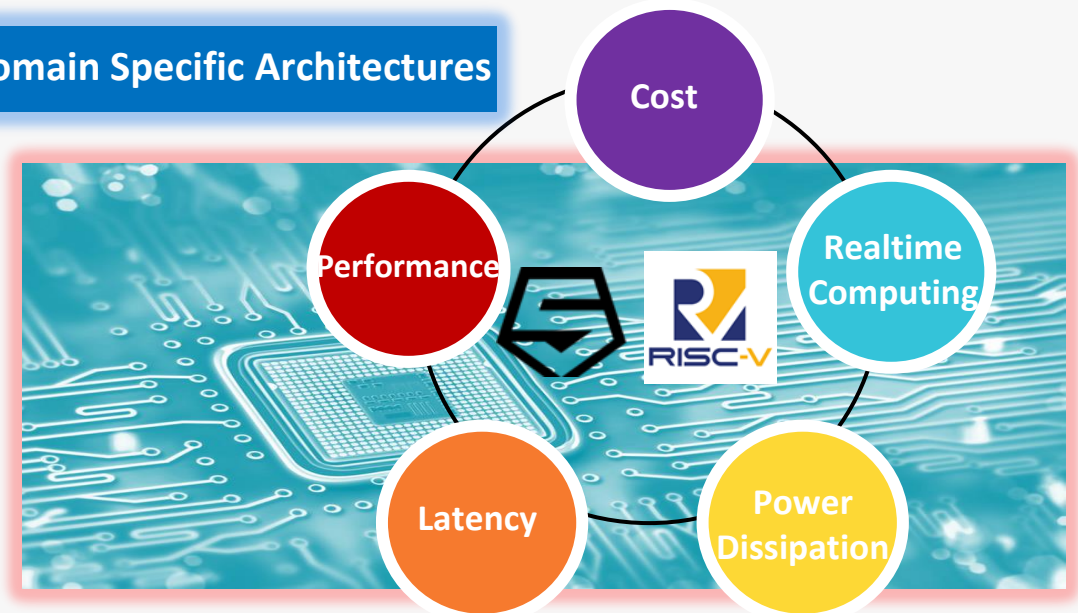
## IOT Drives Edge Computing



## Moore's Law Slowing ....



## Domain Specific Architectures





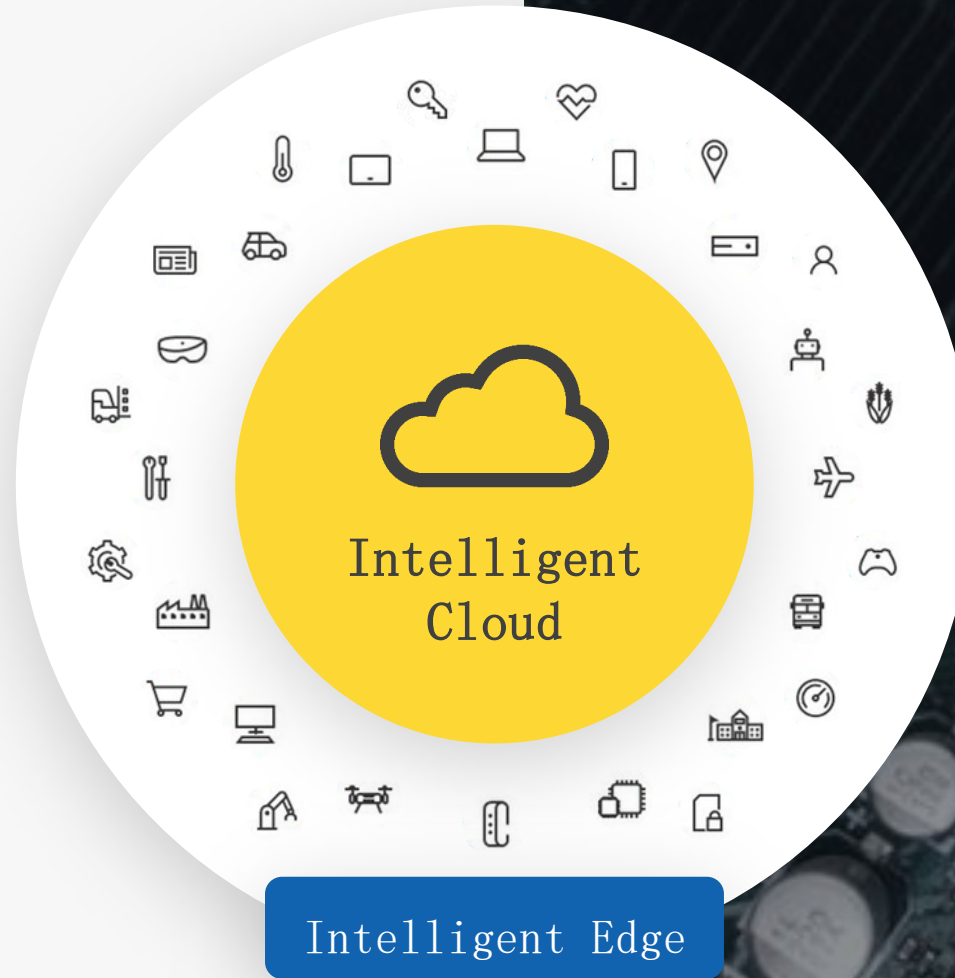
**64-bit Application Processors**



**64-bit Embedded Processors**



**32-bit Embedded Processors**



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**Embedding  
Intelligence  
from the Edge  
to the Cloud**

# SiFive Core IP 2 series:

SiFive's **smallest** and most  
**efficient** RISC-V processor IP



32-bit  
Embedded  
Processors

Efficient RISC-V MCU  
Configurable Core and Memory System  
Ultra low-latency interrupts

Higher  
Performance

Configurable

Low latency  
interrupts

# SiFive Core IP 3 and 5 series:

The **world's most deployed**  
RISC-V processor IP

 E3 Series

32-bit  
Embedded  
Processors

 S5 Series

64-bit  
Embedded  
Processors

 U5 Series

64-bit  
Application  
Processors

**Efficient Performance**  
Coherent, Heterogenous, Multicore  
Hard Real-time capabilities

Configurable

Efficient

Mature

# SiFive Core IP 7 series:

The **highest performance**  
commercial **RISC-V**  
processor IP

 E7 Series

32-bit  
Embedded  
Processors

 S7 Series

64-bit  
Embedded  
Processors

 U7 Series

64-bit  
Application  
Processors

Common Feature sets  
Hard Real-time capabilities  
Unprecedented scalability

~60% increase  
in  
CoreMarks/MHz\*

~40% increase  
in DMIPS/MHz\*

10% increase  
in Fmax\*

\*Compared to SiFive 5  
series

# SiFive 7 Series

## Embedded Intelligence Everywhere

Scalable throughput provided  
by 8+1 cores per cluster

Extensible design via custom  
instructions

Configurable memory  
architecture for application  
specific tuning

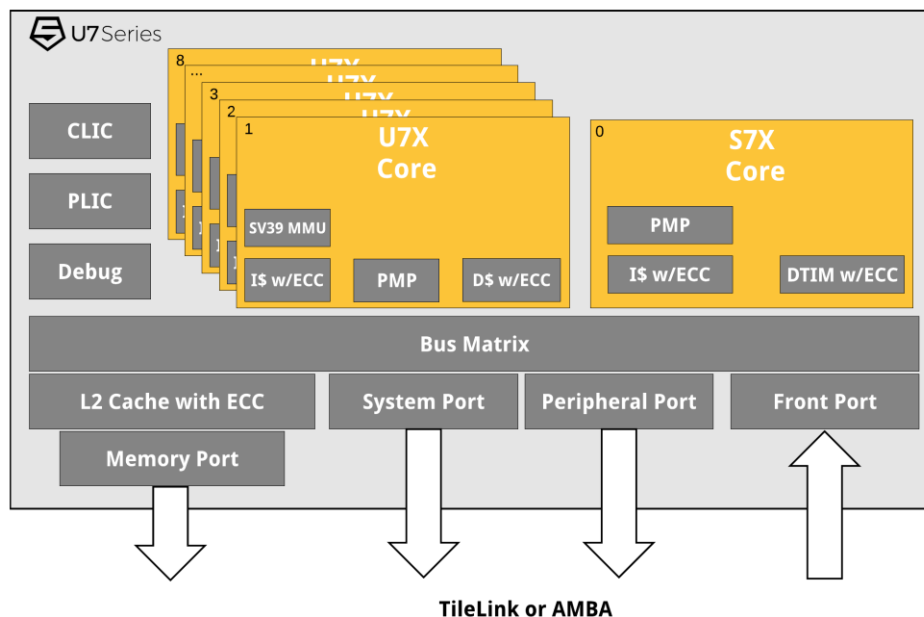
Tightly integrated  
memory for low  
latency access

64-bit addressability  
for real time latency  
sensitive applications

Mixed-precision arithmetic for  
efficient compute of ML  
workloads

Cache lock capability for mission-  
critical computing

In-cluster coherent heterogeneous combination of real-time and application processors



Enhanced determinism for  
hard real-time constraints

Functional safety provided by  
in-built fault tolerance  
mechanisms

A **single** pre-integrated and  
verified deliverable

# Storage

Coherent in-cluster combination of application processors and real-time processors

Deterministic mode for **FAST DATA** applications with hard real-time constraints

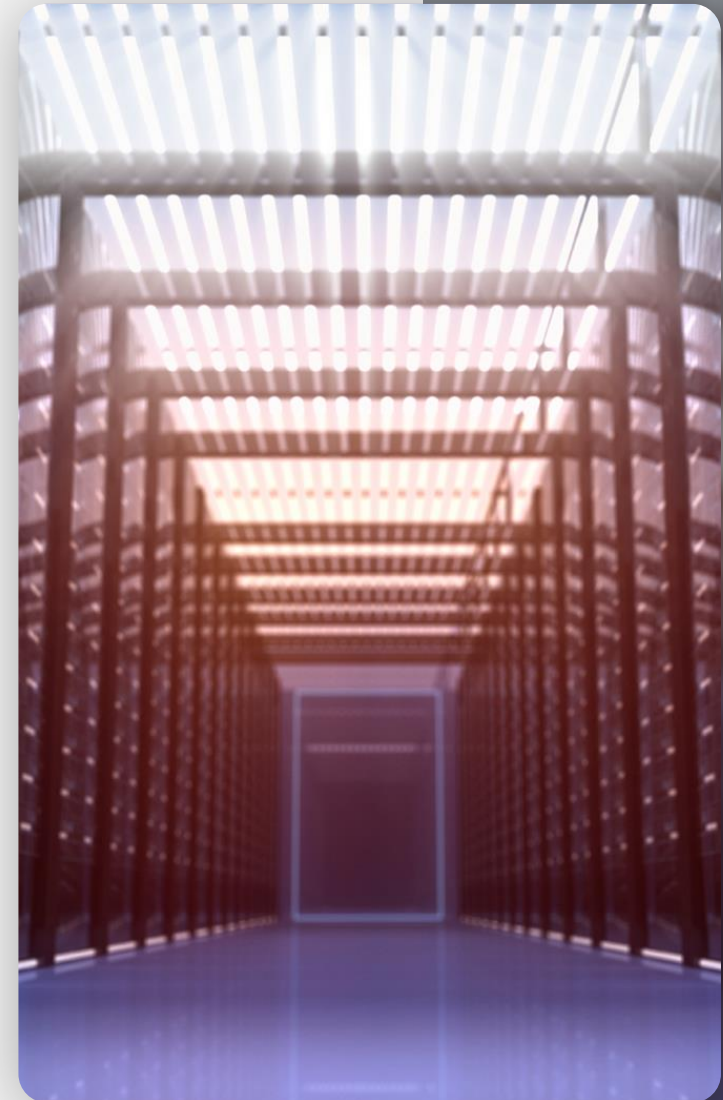
Configurable memory maps and coherent accelerator ports for tightly coupling storage specific accelerators

Tightly integrated memories and Cache lock capability for critical real time workloads

Optional FPU for applications which don't need floating point capability

Storage, ML, Cryptography specific **custom instructions**

64-bit real-time addressability for **BIG DATA** applications



# 5G/Networking

Complex arithmetic capability  
for accelerating baseband  
functions

In-cluster coherence of application  
and real-time processor enables  
5G latency (<1ms) requirements

High bandwidth accelerator ports  
for enabling intelligent offload  
processing

Hard real-time capabilities for  
scheduling baseband protocol  
layers

Configurable memory maps for  
optimizing QoS

High throughput processing for  
next gen 5G stacks

Tightly Integrated Memories and Cache lock capability for  
critical real  
time workloads



# AR/VR/Sensor Fusion

**Low Latency peripheral access** and coherent accelerator port

**Combine** with SiFive 2, 3 or 5 series for designs with tight power constraints

**Coherent in-cluster combination** of application processors with real time processors

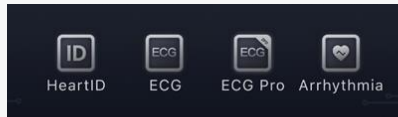
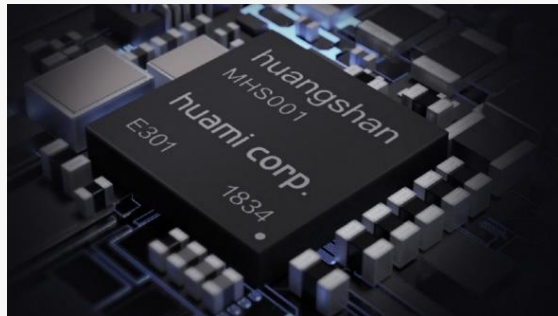
**Workload specific** customizations (AR/VR/MR/CV)

**Simple caching hierarchy** for ease of application optimization

**Mixed precision arithmetic** for accelerating machine learning compute



## Wearable AI

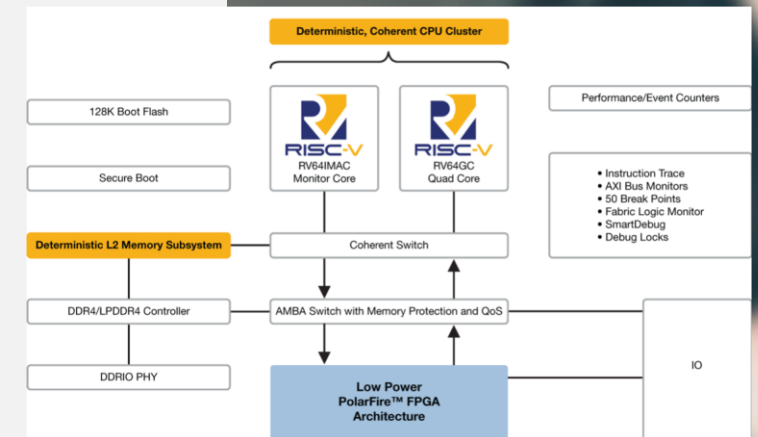


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## Enterprise



## Edge



Rapid adoption of SiFive Core IP from the Edge to the Core

# SiFive Core IP: Embedding Intelligence Everywhere

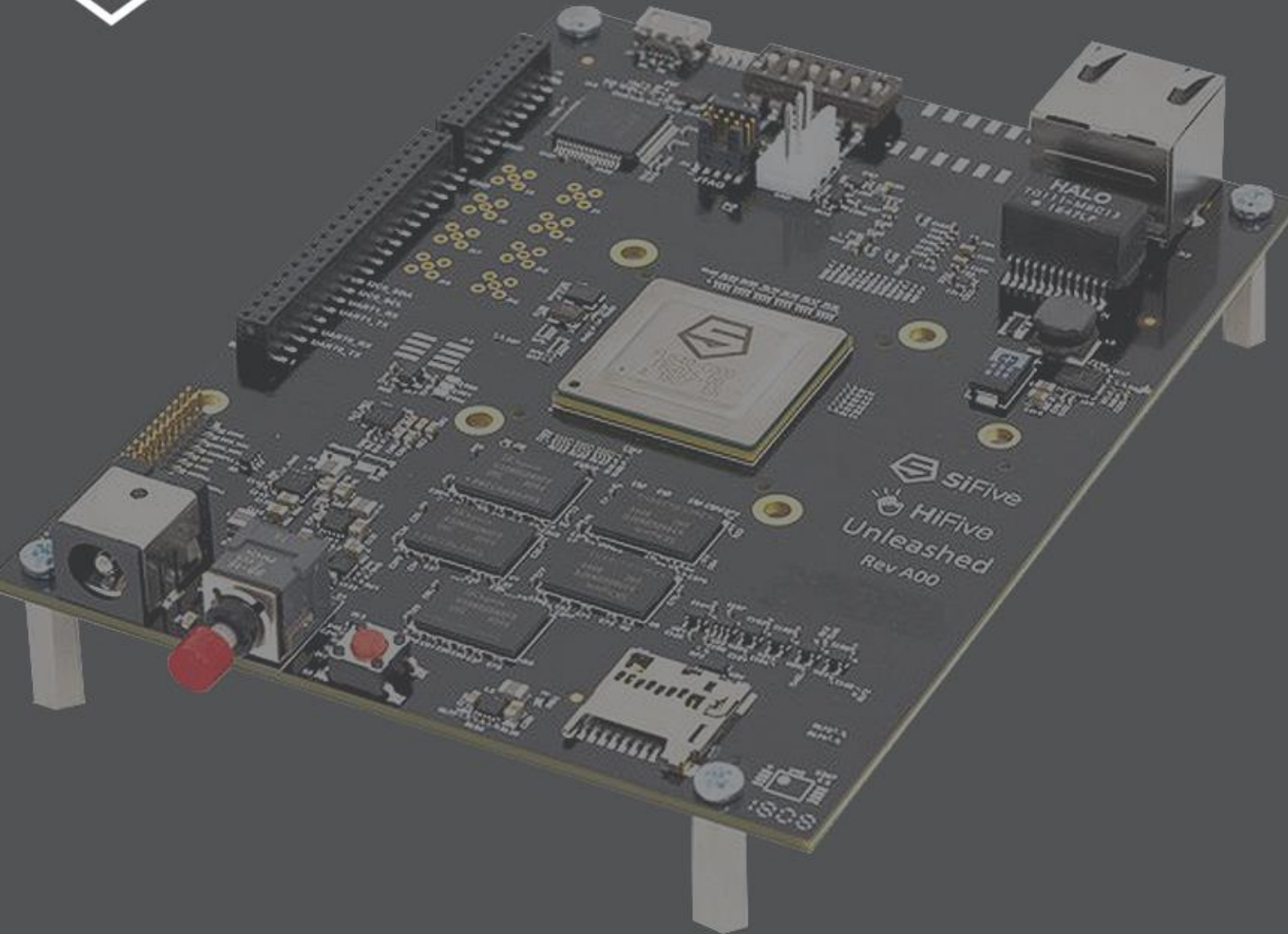
Efficient  
Performance

Scalability

Compelling  
Feature Set



Embedding intelligence  
for a world of a Trillion  
Connected Devices



# Silicon verified. Market proven.

The most advanced configurable core IP and silicon solutions from the inventors of RISC-V.

Microcontrollers ■ Embedded ■ Linux ■ Multicore

■ Networking ■ Storage ■ Computing ■ AI  
■ Industrial ■ IoT ■ Consumer ■ Automotive

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