Microsemi
a Microchip company

Real Time Linux?

Mi-V

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FPGA BU – Embedded Strategy

To be the leading provider of programmable RISC-V solutions

RISC-V

Open. Lowest Power. Programmable RISC-V Solutions

- Highly differentiated, open ISA alternative to ARM
- AMP Mode: Simultaneous Linux + Real Time Flexibility
- Enhances our low power position
- Enhances our security position
- Provenance enables full transparency for trusted design
- A lower cost ASIC migration path than ARM

Key RISC-V Foundation and Industry Partnerships

- MSCC Foundation Board Member: Ted Speers
- MSCC Working Committee Member: Stuart Hoad, Richard Newell
- Strategic Partnership with SiFive
  - Soft 32-bit uCs, Hard Quad-core 64-bit uPs + uC
  - Common MSS architecture, boards, ecosystem

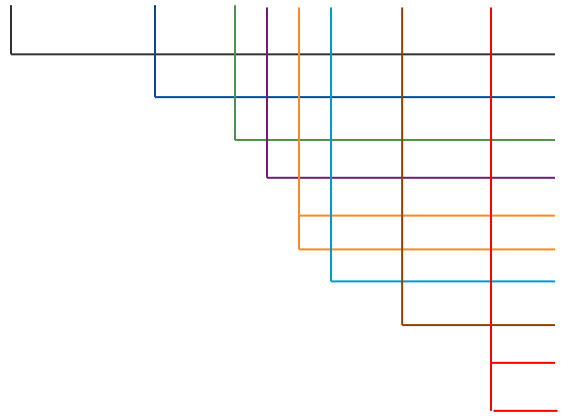
A Comprehensive Ecosystem to Support RISC-V Development

CPUs: Mi-V Soft CPUs & Roadmap

Core	LE's	CoreMark	Cache	Mul/Div	Floating Point	Availability
Mi_V_RV32IMA_L1_AHB	10K	2.01	8K I and D	Yes	N/A	Now
Mi_V_RV32IMAF_L1_AHB	26K	2.01	8K I and D	Yes	Single Precision	Now
Mi_V_RV32I_AHB	5K	-	N/A	N/A	N/A	CQ3'19
Mi_V_RV32IMA_L1_AXI	10K	2.01	8K I and D	Yes	N/A	Now

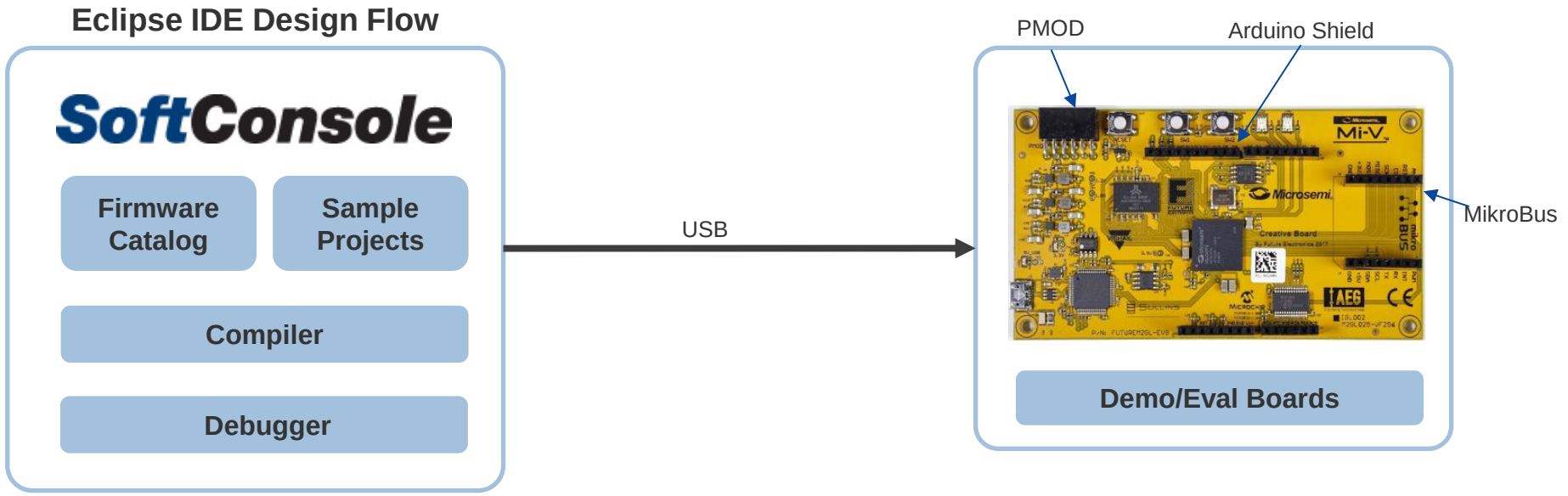
- Mi_V_RV32I_AHB
  - Small core, with/without debug, 5K LE's
- Mi_V_RV32IMA_L1_AHB with SECED available

Mi_V_RV32IMAFC_L1_AHB



Mi-V = Mi-V RISC-V Ecosystem
RV32I = 32 bit integer machine
M = Multiply and Divide
A = Atomic Instructions
F = Single Precision Floating Point
D = Double Precision Floating Point
C = Compressed Instructions
L1 = Instruction and Data Cache
AHB = AHB Bus Interface
AXI = AXI Bus Interface

SoftConsole Eclipse IDE

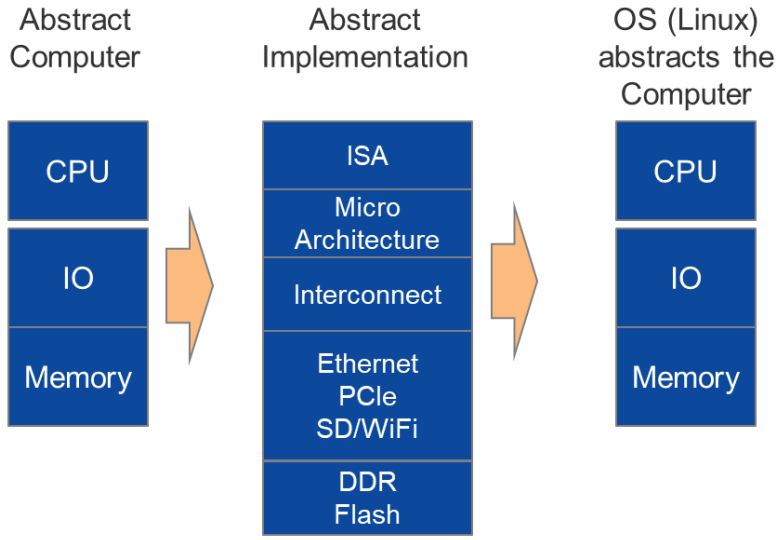


- A single tool chain for RISC-V and ARM MCUs
  - Easy migration from ARM to RISC-V
- Running on Linux or Windows Hosts
- Bundled with example projects and RTOSs

Why RISC-V for a SoC FPGA?

- The RISC-V ISA is Open. Open ISA's allow for …
  - Low cost migration to ASICs, royalty free usage
  - Innovation for custom architectures – free "architectural license" doesn't restrict usage to fixed architectures

- The RISC-V ISA is simple. Simplicity …
  - Allows for a low power implementation
  - Lowers cost of ownership - easier to learn, customize and debug
  - Simple architectures are easier to secure against threats

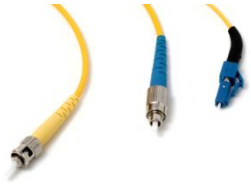


Open, Lowest Power, Cost Optimized, Programmable SoC

PolarFire FPGA Architecture

Open, Lowest Power, Cost Optimized, Programmable SoC

Lowest Power Mid-Range FPGAs

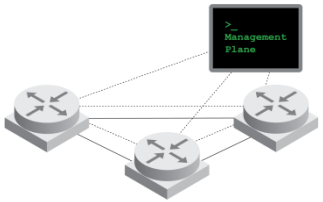


10G Bridging & Aggregation

Microsemi
Power Matters.™

PolarFire™ FPGA

Cost-optimized Lowest Power Mid-range Densities

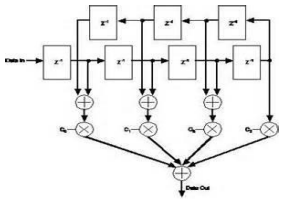


Control Plane (PCIe, GigE, 10GE)

Video & Image Processing

Hardware Acceleration

Portable Communications

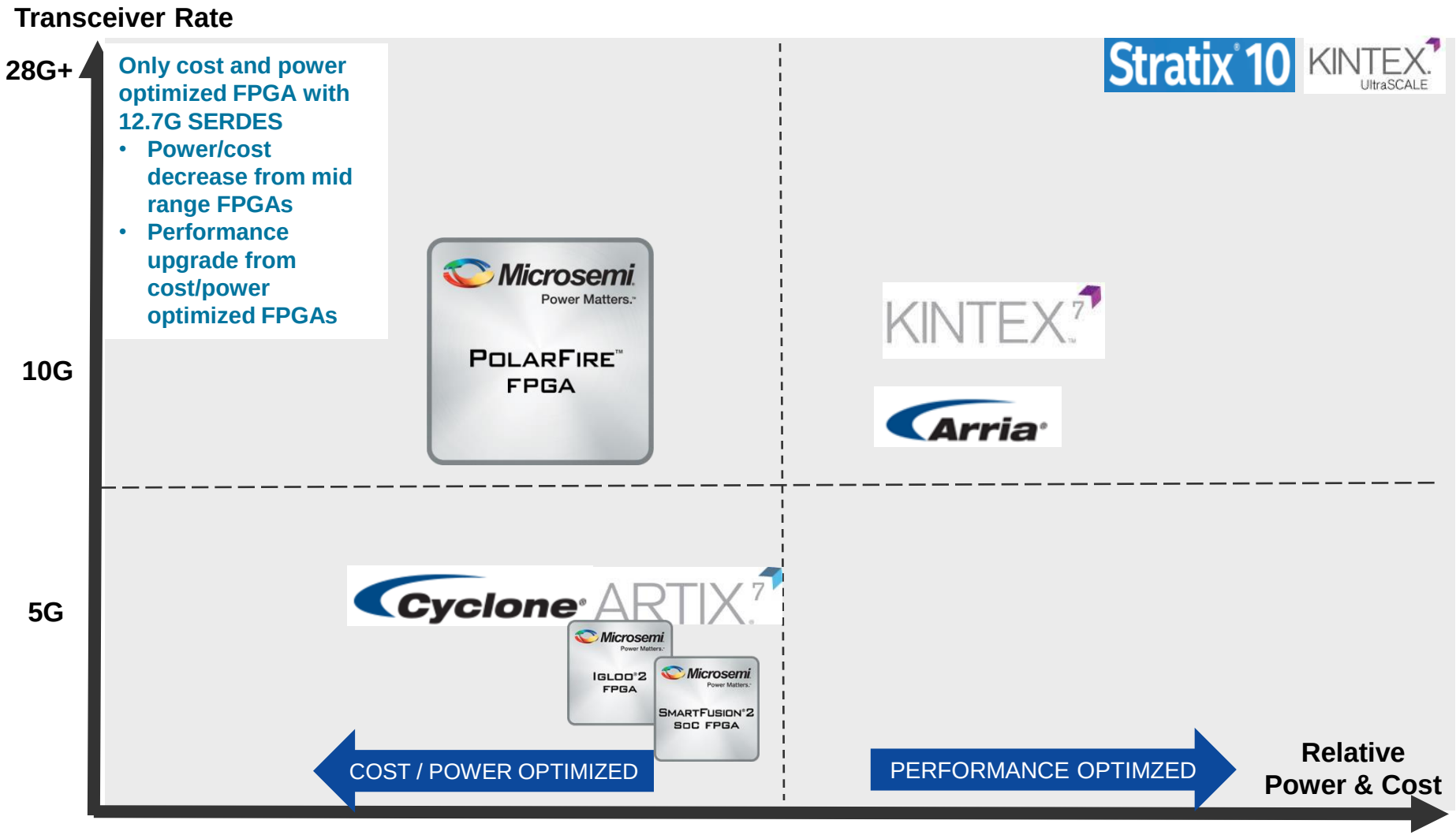


RF and Baseband Signal Processing

Packet Processing & Traffic Management

Low Power Optics

Mid-Range FPGA Landscape



PolarFire FPGAs deliver up to 50% lower power to mid-range

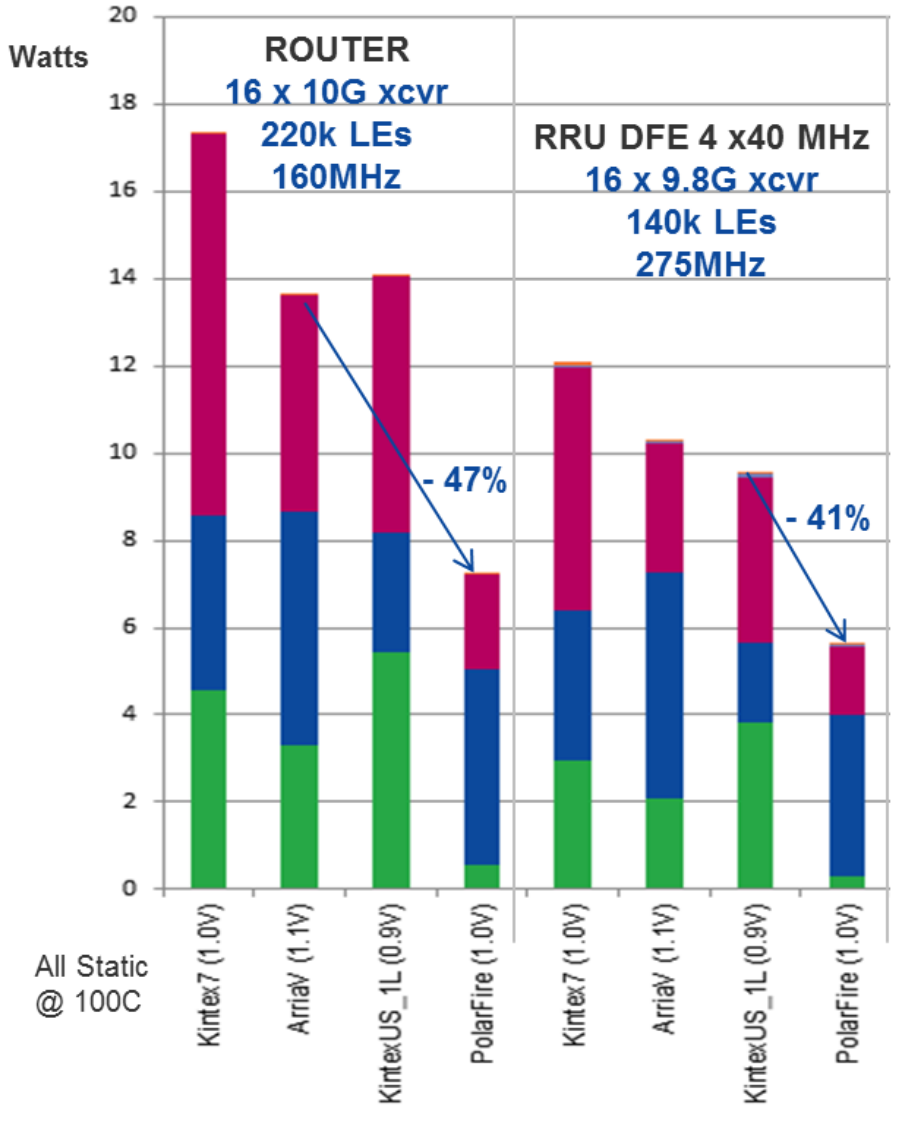
Lowest Power – Save Up to 50%

- Enabling Application Performance at Significantly Lower Power

Static power 10x Reduction

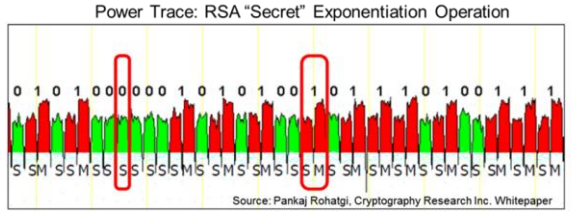
Transceiver 2x Reduction

- ***Total power up to 50% lower than best case competitor number***
- ***PolarFire Customer: $1.5/W in BOM cost saving due to power savings***



Security is All About Layers

To protect your information you need
Secure Hardware, Design Security and Data Security



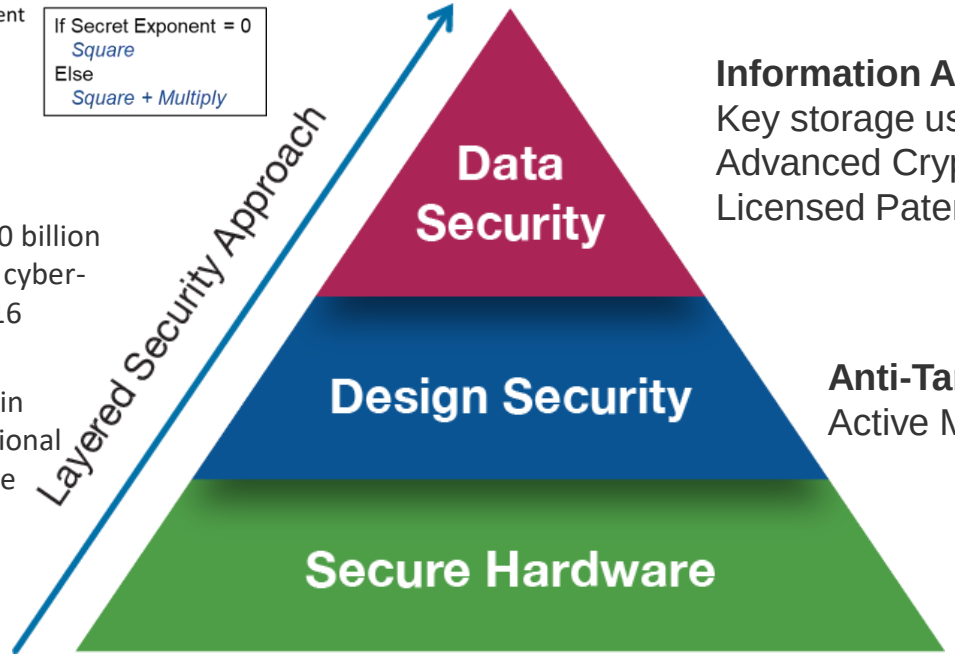
Secret Exponent
{0 or 1}

S = Square
M = Multiply

If Secret Exponent = 0
Square
Else
Square + Multiply

"The number of IoT sensors is expected to approach 30 billion in 5 years – and each unit is a potential entry point for cyber-criminals" – The Economist Intelligence Unit, 4/11/2016

"Some call cybercrime the greatest transfer of wealth in human history" – The Center of Strategic and International Studies, July 2013, The Economic Impact of Cybercrime



Information Assurance:
Key storage using Physically Unclonable Function (PUF)
Advanced Crypto Accelerators
Licensed Patent Protected DPA Resistance Pass through License

Anti-Tamper: Secure Bitstream, Tamper Detection, Active Mesh, No Copying. Cloning, or Reverse Engineering

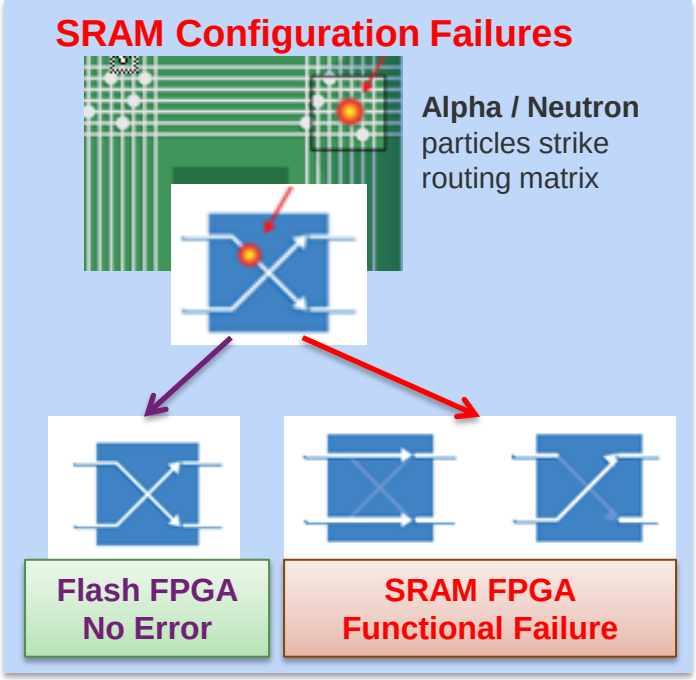
Trust: Licensed Patent Protected DPA Resistance, NIST Certified Crypto Accelerators, Secure Supply Chain

LICENSED DPA COUNTERMEASURES™

Microsemi FPGAs provide a solid foundation for your security needs

Exceptional Reliability

- Error Free SEU immune Fabric Configuration
  - No need to detect configuration errors
    - No scrubbing required
    - No triple mode redundancy needed
    - Lowers cost
- Memories are also protected
  - Built-in SECDED on 33 bit word
- System Controller Suspend Mode for Safety Critical Applications



SEU a growing concern for equipment demanding 99.999% uptime

PolarFire Product Family

	Features	PolarFire FPGA			
		MPF100	MPF200	MPF300	MPF500
FPGA Fabric	Logic Elements (4LUT + DFF)	109K	192K	300K	481K
	Math Blocks (18x18 MACC)	336	588	924	1480
	LSRAM Blocks (20 kbit)	352	616	952	1520
	uSRAM Blocks (64x12)	1008	1764	2772	4440
	Total RAM (Mbits)	7.6 Mbits	13.3 Mbits	20.6 Mbits	33 Mbits
	uPROM (kbits	297 Kbits	297 Kbits	459 Kbits	513 Kbits
	User DLL's/PLL's	8 each	8 each	8 each	8 each
High Speed I/O	250 Mbps -12.7 Gbps Transceiver Lanes	8	16	16	24
	PCIe Gen2 Endpoints/Root Ports	2	2	2	2
Total I/O	Total User I/O	284	364	512	584
Packaging	Type / Size / Pitch	Total User I/O (HSIO / GPIO) GPIO CDRs / XCVRs			
	FCSG325 (11x11, 11x14.5*, 0.5 mm)	170(84/86) 8/4	170(84/86) 8/4*		
	FCSG536 (16x16, 0.5 mm)		300(120/180) 15/4	300(120/180) 15/4	
	FCVG484 (19x19, 0.8 mm)	284(120/164) 14/4	284(120/164)14/4	284(120/164) 14/4	
	FCG484 (23x23, 1.0 mm)	244(96/148) 13/8	244(96/148) 13/8	244(96/148) 13/8	
	FCG784 (29x29, 1.0 mm)		364(132/232) 20/16	388(156/232) 20/16	388(156/232) 20/16
	FCG1152 (35x35, 1.0 mm)			512(276/236) 24/16	584(324/260) 24/24
		Devices in the same package and family type are pin compatible			

Extended Commercial (0ºC-100ºC) and Industrial (-40ºC-100ºC) Temperature Support for all Die Package Combinations - RoHS only

Additional Temp Grade: Military (-55ºC-125ºC) - Leaded packages only

Note: FC484M package is a lidded package whereas the FCG484I package is not.

PolarFire SoC Architecture

Open, Lowest Power, Cost Optimized, Programmable SoC

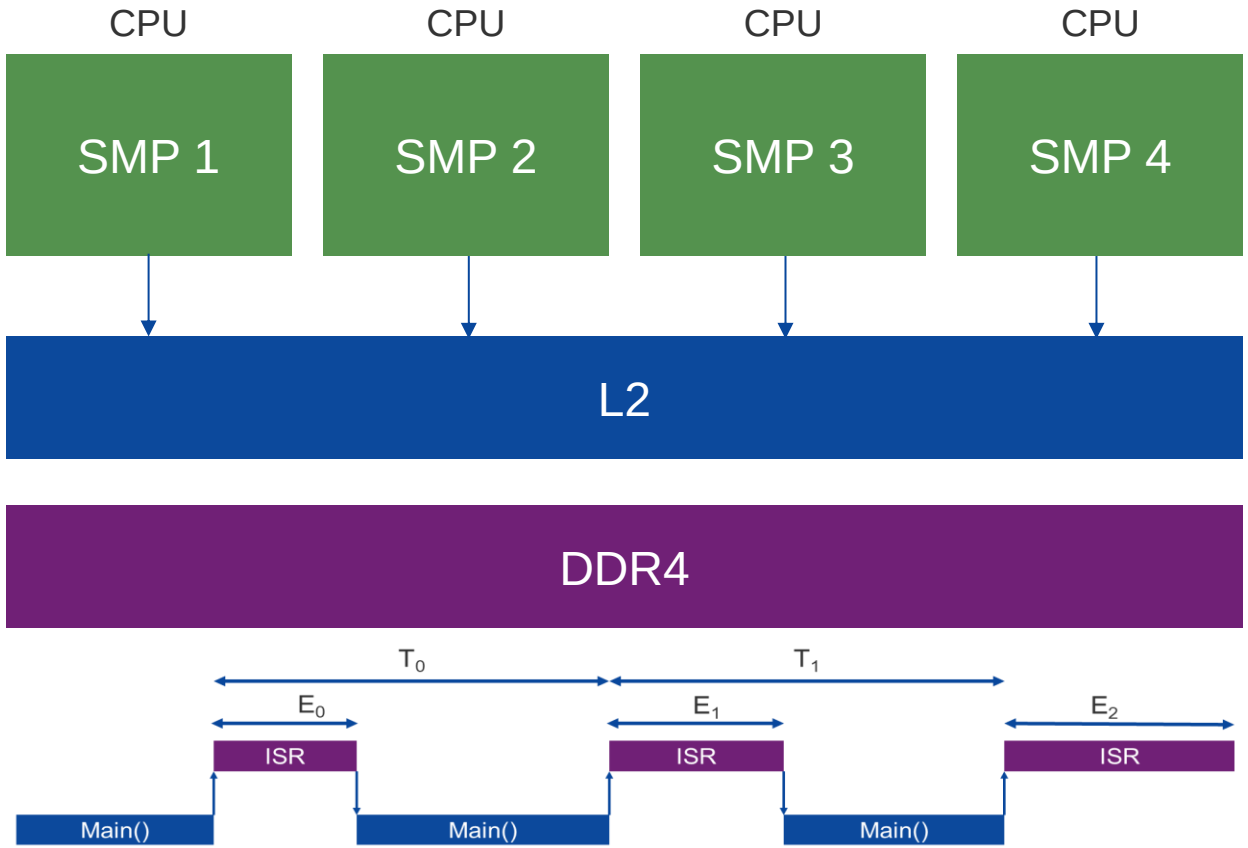
Real-time Linux?

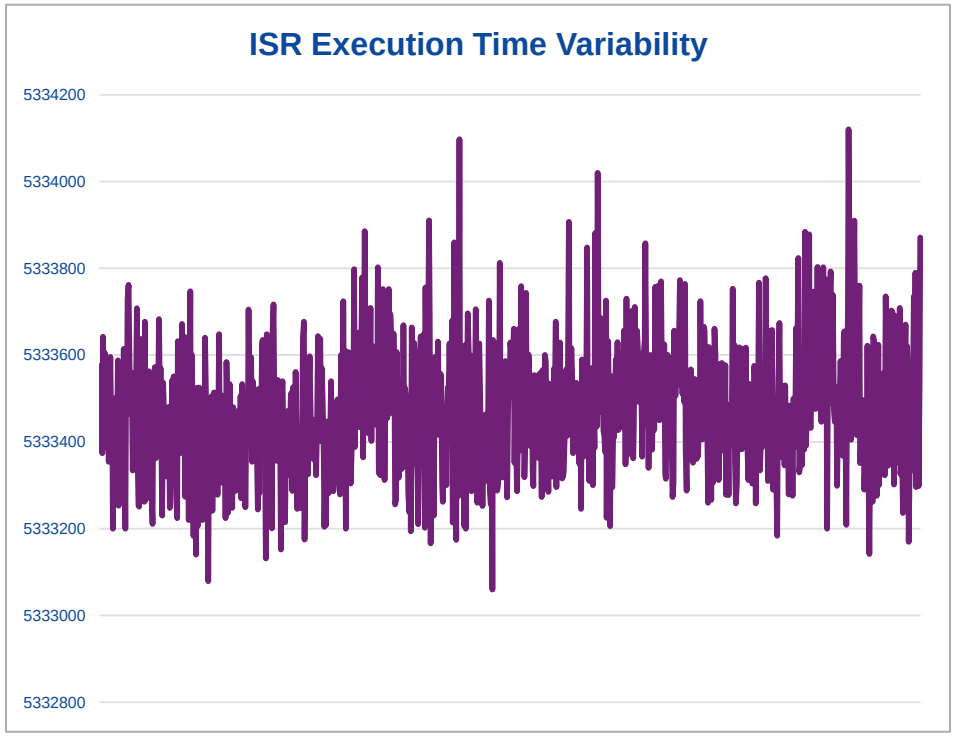
- Wide spread Linux adoption
  - Rich OS with thousands of applications to choose from

- Requirements still exist for real-time while running Linux
  - Safety critical
    - The ability to deterministically monitor the execution environment.
  - Real-time system control
    - Completing tasks deterministically, on time every time.
  - Securing the IoT
    - Execute a trusted execution environment deterministically for consistent results.

- Working with our partner SiFive
  - We have been able to architect a complex SoC FPGA that provides
    - Determinism and a rich OS within the same multi-core CPU cluster

Variable Execution Time in Typical Application Processors



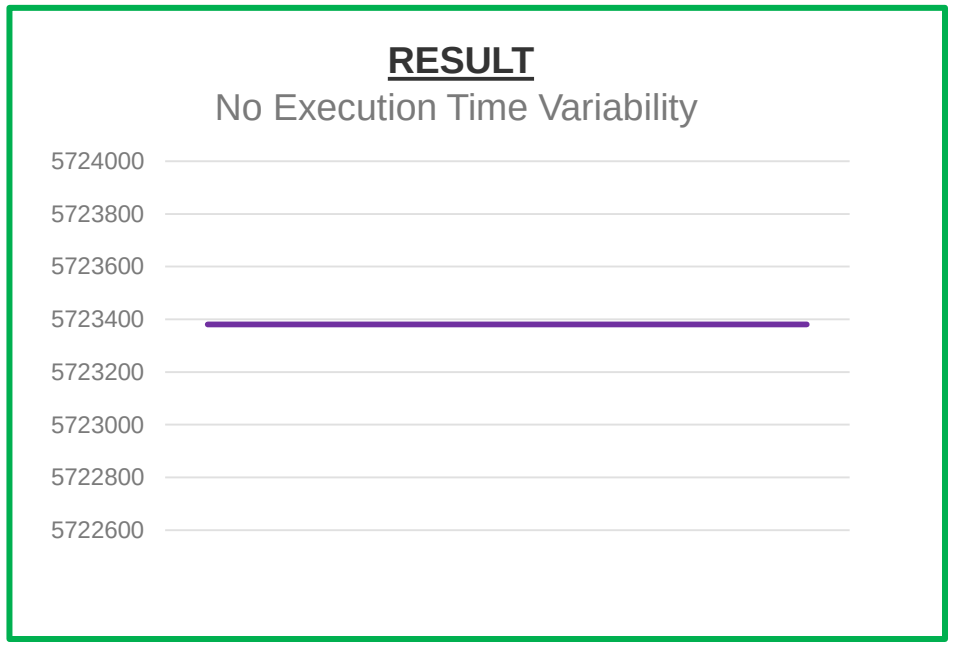


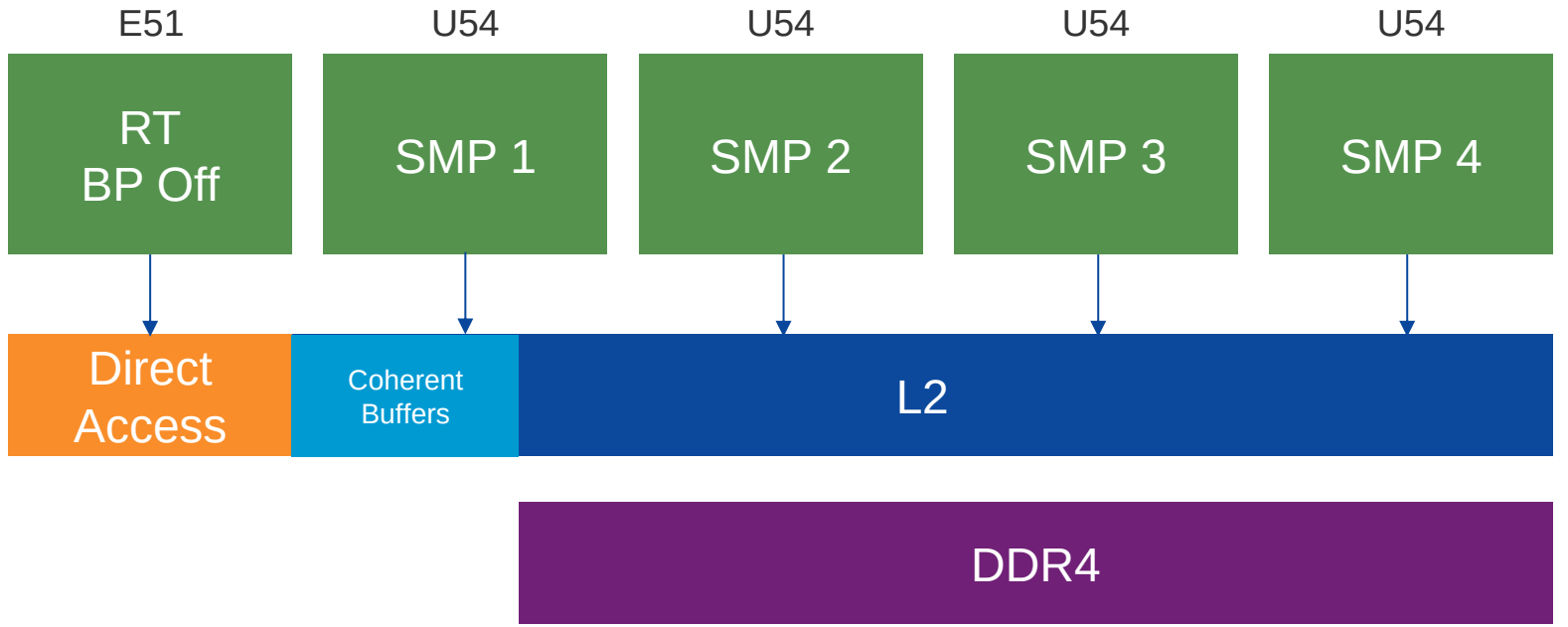
- Periodic Interrupts
  - $T_0 = T_1$
- Inconsistent Execution Times
  - $E_0 != E_1 != E_2$

Branch predictors, cache misses and lack of coherency ***affect determinism negatively***

Real-Time and Linux

- Turn off the CPU branch predictors
- Convert L1 to Tightly Integrated Memory
- Make sure all cores coherent to the memory subsystem
- Make the memory system deterministic
- Share coherent memory for message passing

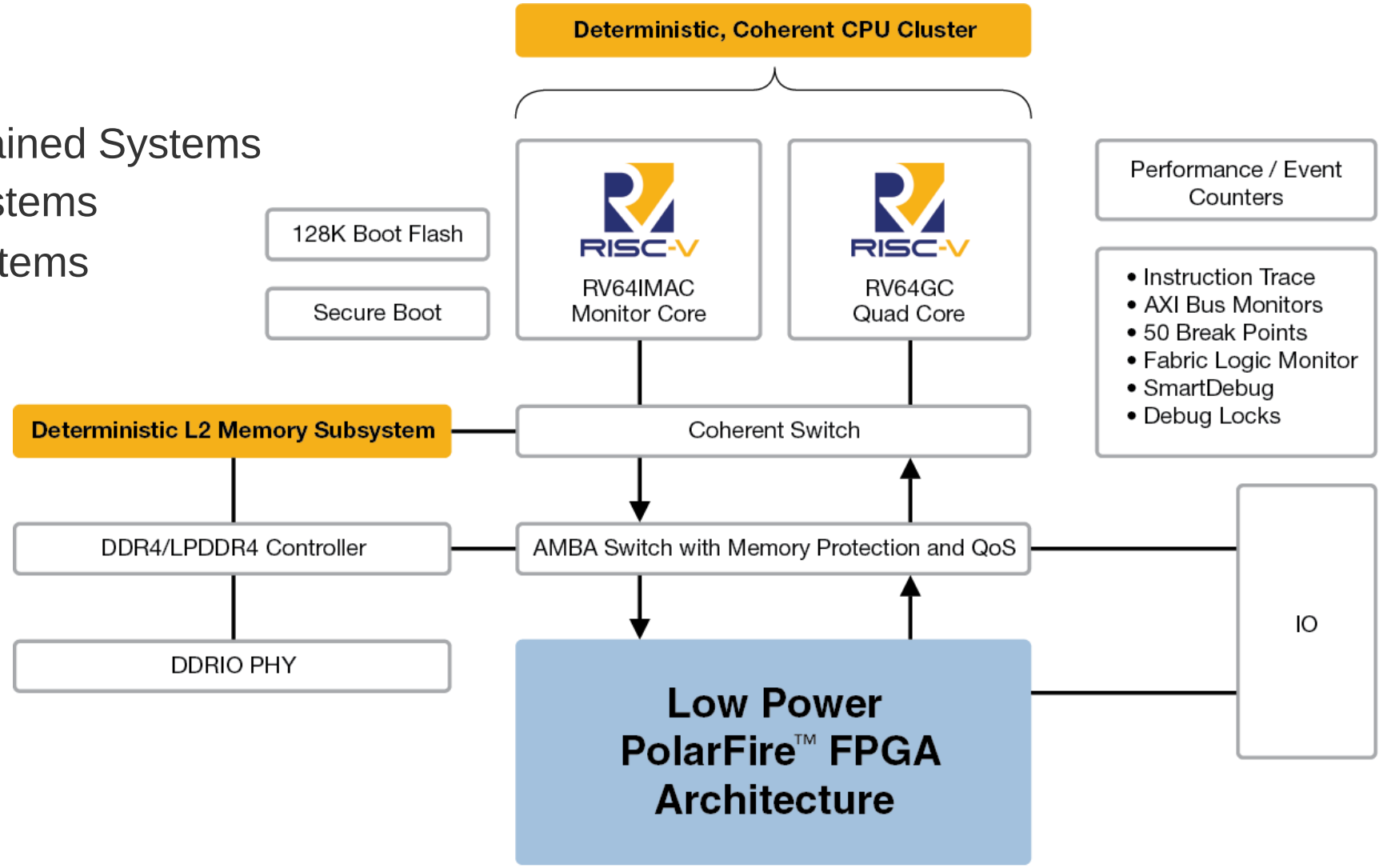




PolarFire SoC - RISC-V enabled innovation platform

Freedom to Innovate in

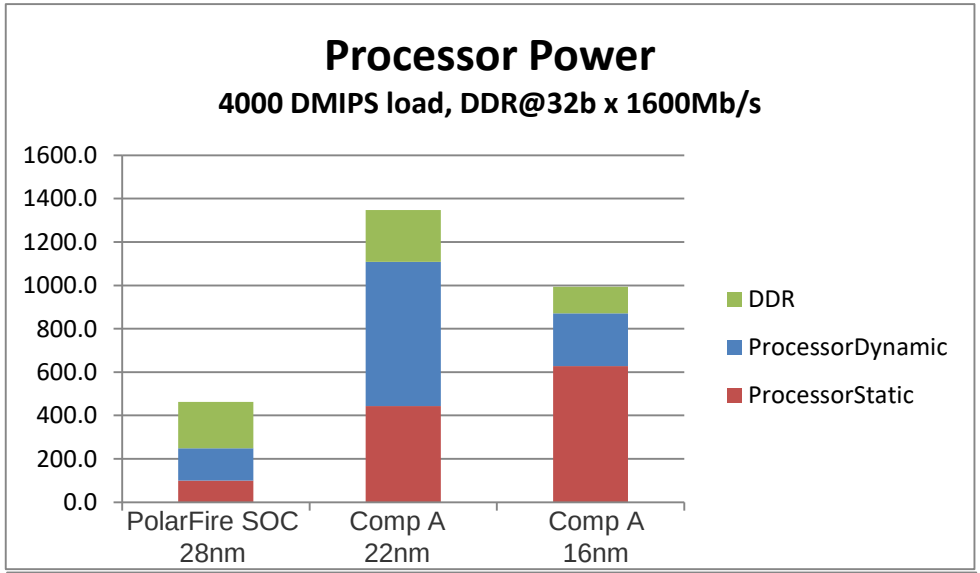
- Linux and Real-Time
- Thermal and Power Constrained Systems
- Securely Connected IoT systems
- High-Rel Safety Critical Systems



SiFive

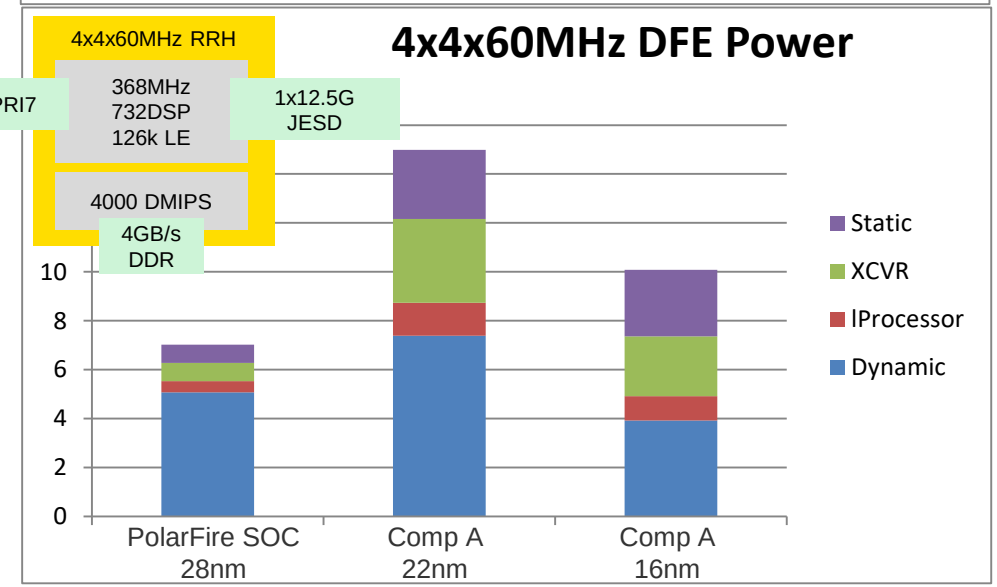
ultraSoC

Low Power: RISC-V MSS vs. Alternatives



Low Power MSS

- Low power RISC-V micro-architecture
- 2MB L2 cache: increases cache hit/miss ratio
- 0.5-0.9W lower power



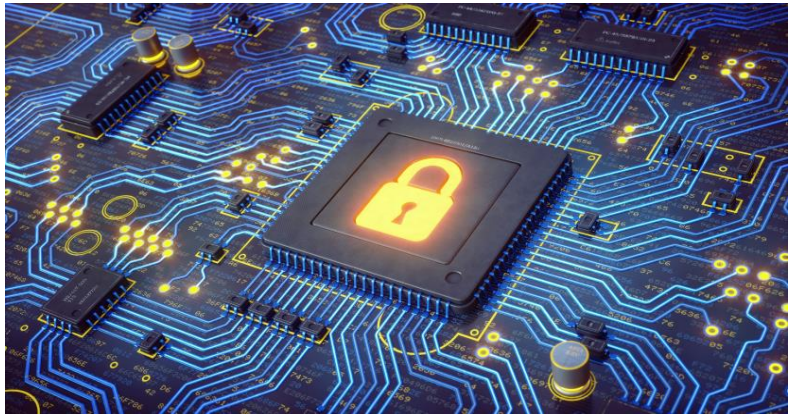
LTE Digital Front End Application

- 3-7W lower power for 60MHz 4x4 MIMO implementation

Security Built for Defense, Ready for IoT

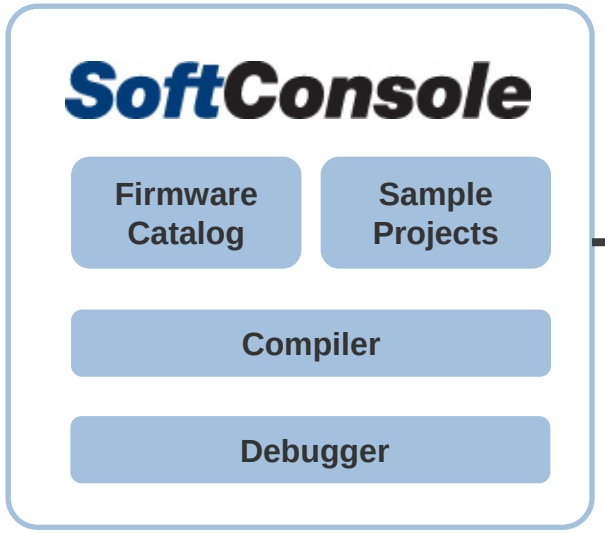
- PolarFire SoC inherits best in class PolarFire FPGA Security
  - DPA resistant bitstream programming
  - Anti-tamper
  - Cryptographical bound supply chain assurance
  - Physically unclonable function
  - True random number generator
  - Side channel resistant crypto coprocessor

- **PolarFire SoC has:**
  - + **Secure Boot**
  - + **Spectre and Meltdown immunity**
  - + **Physical memory protection**
  - + **SECDED on all memories**



Pre-silicon PolarFire SoC Development Options

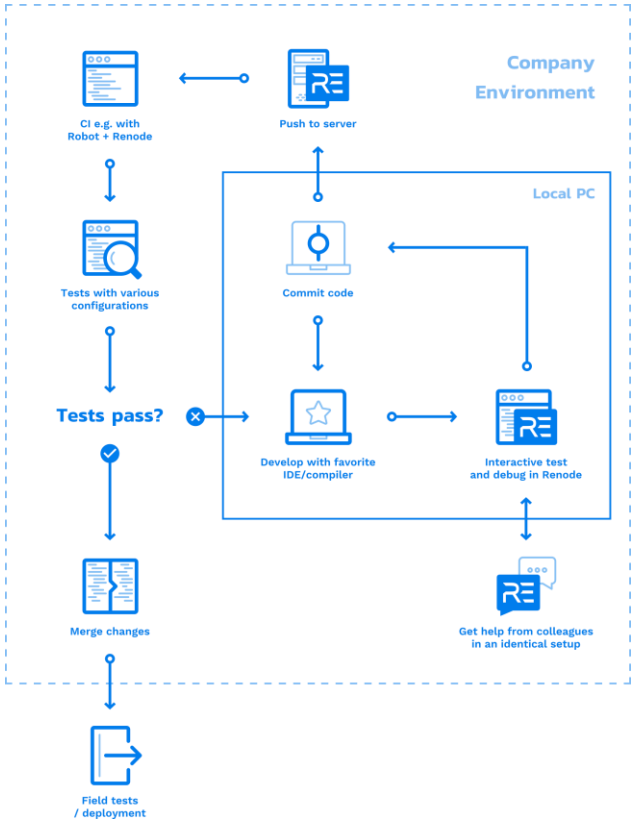
Freedom to start software development



Eclipse IDE Design Flow

GDB

RENODE™

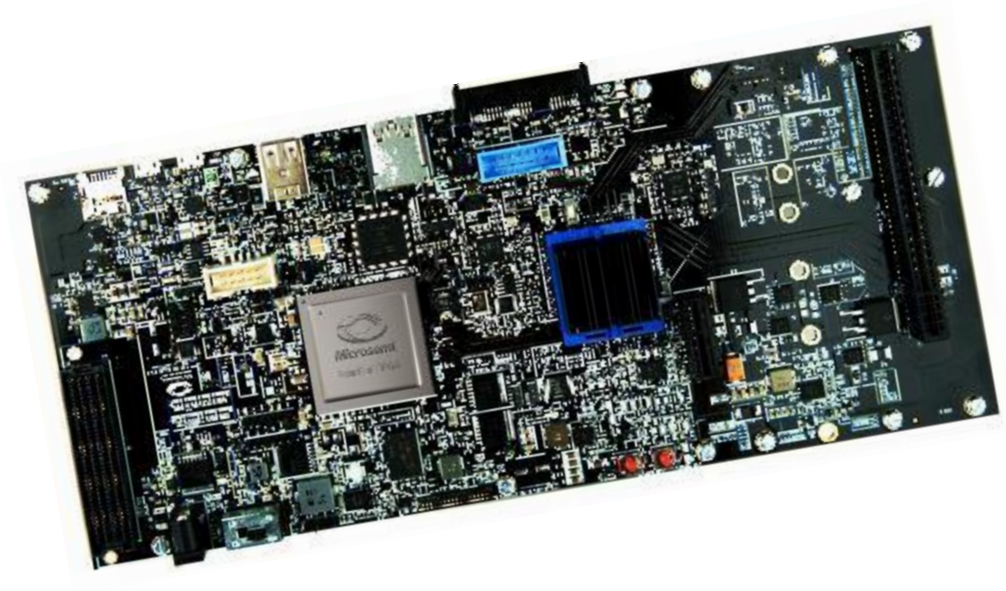


- Free Rapid Software Development and Debug Capabilities Without Hardware
- Complete PolarFire SoC Processor Subsystem Model
- Available now

antmicro

Freedom to begin hardware development

PolarFire SoC Embedded Experts Development Kit



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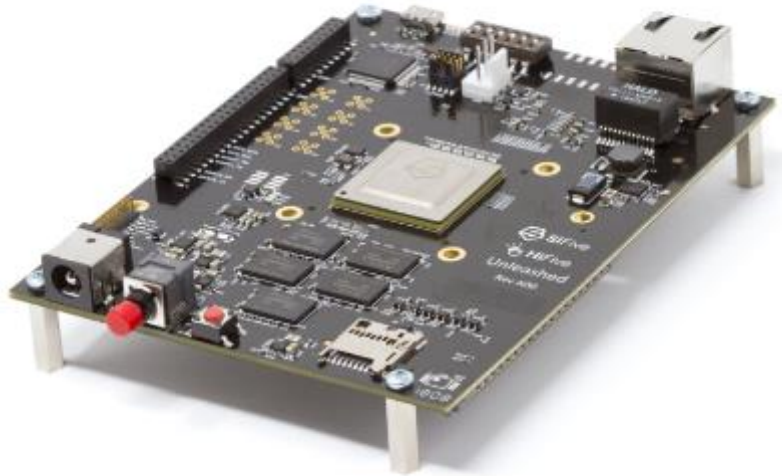

HiFive Unleashed Expansion Board

HiFive Unleashed Development Board

Microsemi
a Microchip company

MPFS-DEV-KIT

SiFive

PolarFire SoC Summary

- PolarFire FPGA Award Winning Features
  - 30-50% Lower power
  - Defense grade security
  - Exceptional reliability
  - Smallest, lowest power, secure form factors – 11x11, 16x16, 19x19

- PolarFire Microprocessor Subsystem
  - Linux and real time in a deterministic, coherent CPU cluster
  - 30-50% Lower power
  - Defense grade secure boot
  - Spectre/Meltdown immune
  - SECDED on all memories

Click here to learn more

Demo

TinyYOLOv2 benchmark demo on MPF300T & RISC-V
- Performance 43.6fps at 304 GOPS
- Power consumption 2.98W (Core)
- Resources used ~200K LE

Input image shape	416 x 416
Number of convolutional layers	9
GOPs (MULACC)	7

Thank You

kk@microchip.com

Open, Lowest Power, Cost Optimized, Programmable SoC