

THE RISC-V[®] FOUNDATION

Krste Asanovic
Chairman of the Board,
RISC-V Foundation



@risc_v



What is RISC-V

- Free and Open Hardware Instruction Set Architecture (ISA)
- Started in 2010 at UC Berkeley
- Frozen base user spec released in 2014
- Fifth major RISC ISA design effort out of Berkeley

It is a Revolution!!





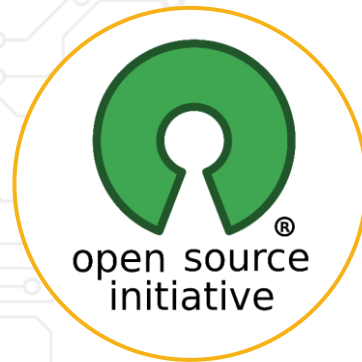
Why RISC-V



Legacy ISA's Are
Decades Old



RISC-V Unlocks the
Architecture & Enables
Innovation



RISC-V is License-Free,
supports Open-Source



RISC-V Ecosystem

Open-source software:

Gcc, binutils, glibc, Linux, BSD,
LLVM, QEMU, FreeRTOS,
ZephyrOS, LiteOS, SylixOS, ...

Commercial software:

Lauterbach, Segger, Micrium,
ExpressLogic, Ashling, Imperas,
...

Software



ISA specification

Golden Model

Compliance

Hardware

Open-source cores:

Rocket, BOOM, RI5CY,
Ariane, PicoRV32, Piccolo,
SCR1, Swerv, Hummingbird,
...

Commercial core providers:

Andes, Bluespec, Cloudbear,
Cudasip, Cortus, C-Sky,
Nuclei, SiFive, Syntacore, ...

Inhouse cores:

Nvidia, +others



Benefits of RISC-V

Simple

Stable

Modular

Designed for
Extendability/
Specialization

Clean-Slate
Design





Why is RISC-V so popular?

- Engineers sometimes “*don’t see forest for the trees*”
- The movement is ***not*** happening because some benchmark ran 10% faster, or some implementation was 30% lower power
- The movement ***is*** happening because ***new business model*** changes everything
 - Pick ISA first, then pick vendor or build own core
 - Add your own extension without getting permission
- Implementation features/PPA will follow
 - Whatever is broken/missing in RISC-V will get fixed



The RISC-V Foundation—Today

A non-profit corporation governed by an elected board of directors

- Develop, ratify, and maintain the RISC-V ISA and related specifications
- Grow Membership
- Create awareness





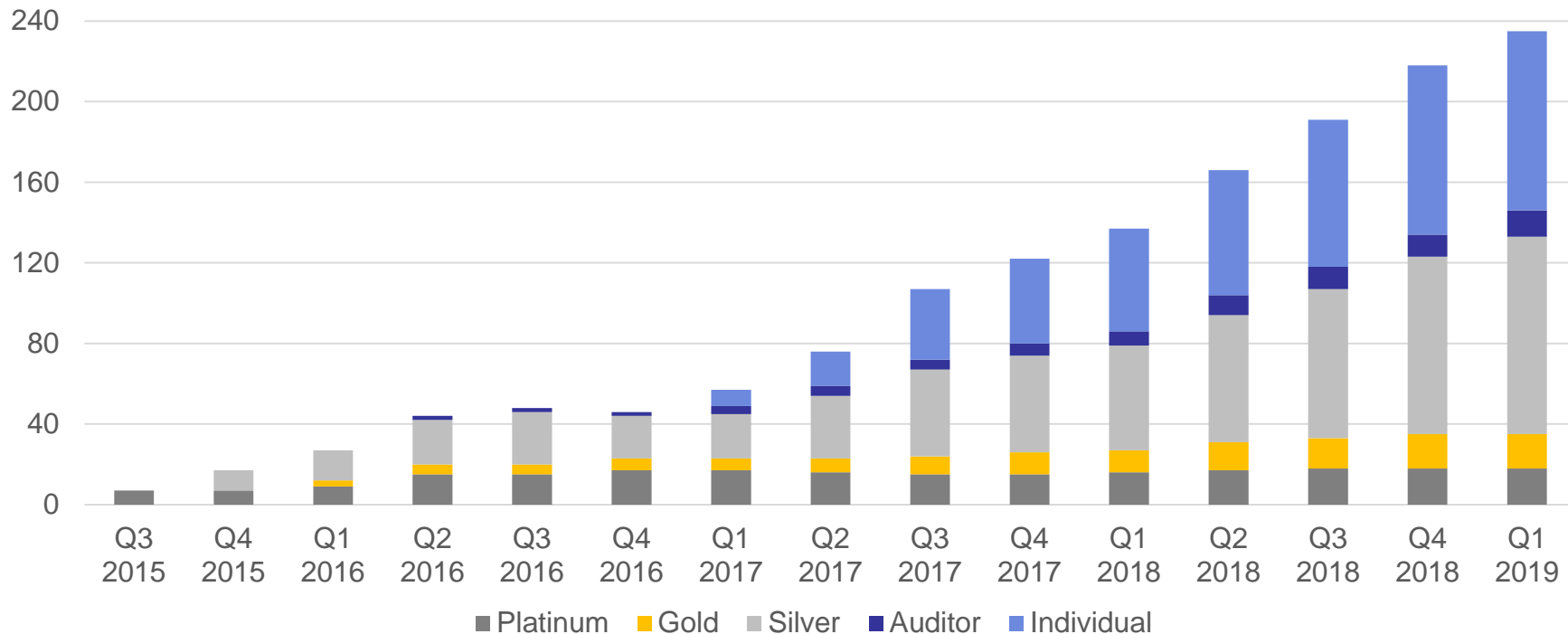
RISC-V Foundation Board of Directors

- Krste Asanović, Chairman
 - Professor in the EECS Department at **UC Berkeley**, Chief Architect, **SiFive**
- David Patterson, Vice-Chairman
 - **Google** Architect, Retired Professor Computer Science UC Berkeley
- Zvonimir Bandić
 - Senior Director of Next Generation Platform Technologies at **Western Digital** Corporation
- Charlie Hauck
 - CEO of **Bluespec** Inc.
- Rob Oshana
 - Director Global SW Development at **NXP**
- Frans Sijstermans
 - Vice President Engineering at **NVIDIA**
- Ted Speers
 - Technical Fellow, Head of Product Architecture for **Microsemi** SoC Group



RISC-V Foundation Growth

September 2015 – February 2019







Meetups (1,500+ Members)

Grass-Roots Effort

Bay Area RISC-V Group

<https://www.meetup.com/Bay-Area-RISC-V-Meetup/>

Rocky Mountain Area RISC-V Group

<https://www.meetup.com/Rocky-Mountain-Area-RISC-V-Group/>

Austin Area RISC-V Group

<https://www.meetup.com/Austin-Area-RISC-V-Group/>

Israel RISC-V Meetups

<https://www.meetup.com/Israel-RISC-V-meetups/>

Cambridge RISC-V Meetup Group

<https://www.meetup.com/Cambridge-RISC-V-Meetup-Group/>

Bristol RISC-V Meetup Group

<https://www.meetup.com/Bristol-RISC-V-Meetup-Group/>

Pune RISC-V Group

<https://www.meetup.com/Pune-RISC-V-Group/>

Vienna RISC-V Meetup

<https://www.meetup.com/Vienna-RISC-V-Meetup/>

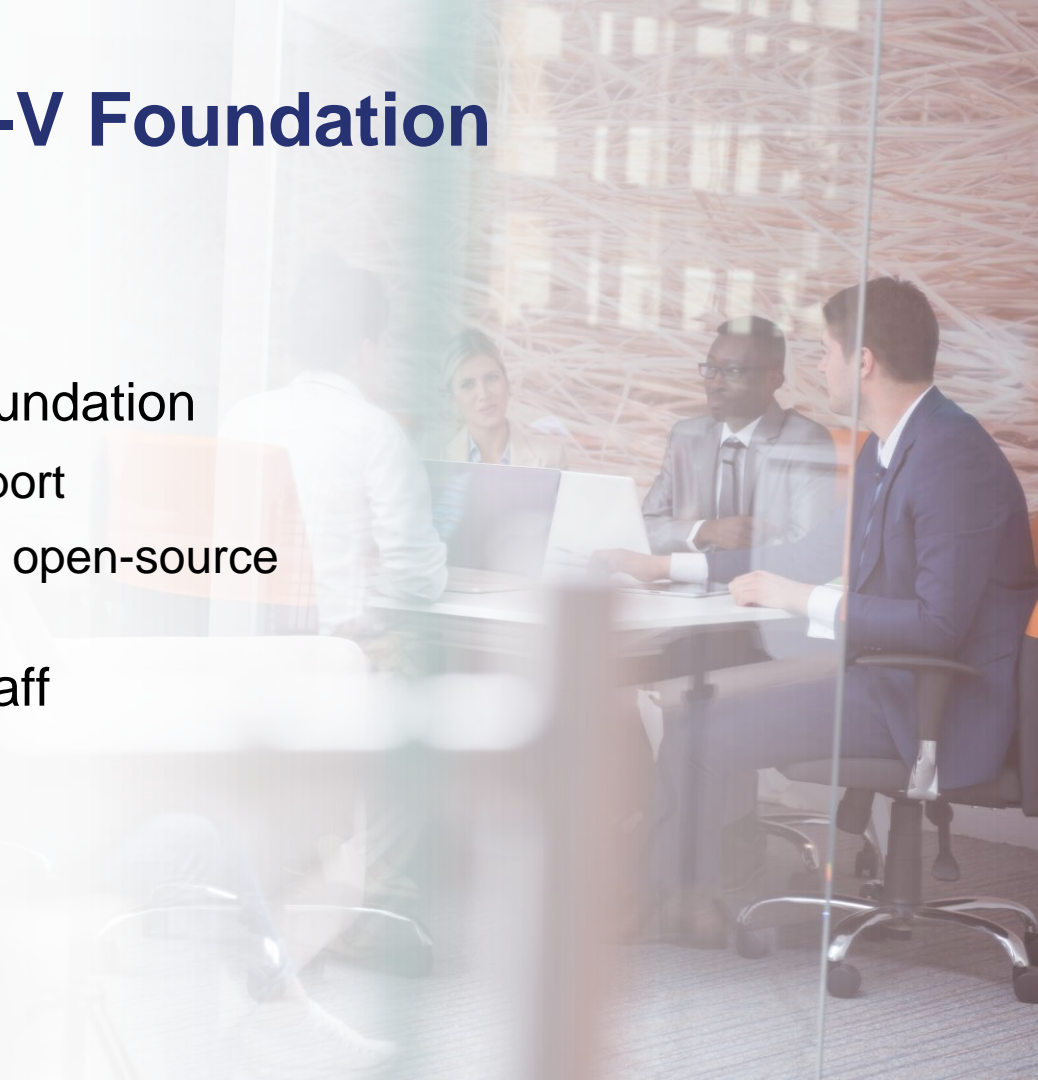
Shanghai RISC-V Meetup

<https://www.meetup.com/shanghai-riscv/>



Scaling the RISC-V Foundation

- Newly created CEO position
- Partnership with the Linux Foundation
 - Leverage services and support
 - Enable synergies with other open-source organizations
- Addition of more dedicated staff





Calista Redmond, CEO



Previously, Vice-President of
IBM Z Ecosystem division;
President of OpenPOWER
Foundation.



Areas of Focus Going Forward

**Standards /
Specifications**

Ecosystem Growth

Member Growth

Compliance

Awareness

Education

Investor Community

Country Adoption

Research

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Standards Development

- Unprivileged base and initial extensions now formally ratified
 - RV32IMFDC, RV64IMFDC
 - "A" extension has one minor issue to resolve (LR/SC progress)
 - User ISA stable since 2014 release
- Privileged spec passed public review for ratification
- Multiple Formal models available
- Vector specification 0.7 released as stable draft in January 2019
 - Largest single extension to date
 - Target of advanced implementation work
- Other new ISA modules in advanced development:
 - Fast interrupts, DSP, Bit manipulation, Hypervisor, ...
- Member-driven ISA roadmap

Foundation Working Groups (partial list)



Bit Manipulation



Compliance



Debug



Memory Model



Privileged Spec



Vector



Security



Base ISA /
Opcode

Fragmentation versus Diversity

- Fragmentation, doing the same thing in multiple different ways
- Diversity, supporting many use cases
 - RISC-V designed to be modular, support specialization
 - Especially important in embedded applications



Ecosystem Growth

Foundries

**Compilers /
SW Dev Tools**

**EDA Tools / Design
Enablement**



**IP Block
Portfolios**

OS Support

Simulators



Raising Awareness



1 Major Annual Summit (San Jose) + 2 Workshops (Zurich & Taiwan)

- Expecting to grow the number and size



15 One-Day events

- US (Milpitas, Irvine, Austin, Boston)
- China (Beijing, Shanghai, Hanzhou, Shenzhen, Chengdu)
- Europe (UK, Munich, Berlin, Paris, Tel Aviv, Estonia)



Sponsored webinars



Continue working with members on grass root initiatives

- Meetups
- ***Member-held events***



Education



Develop Education Resources At All Levels



Drive Adoption By Universities



Develop Corporate Education Partnership Programs to Reach Students Globally



Drive the Development of Low Cost Boards



Develop a Training Certification Program



Develop Online Training Modules





Value Proposition for Members

- Ability to drive standards and set direction on future specifications
- Use of the RISC-V trademarks and logos
- Several RISC-V Foundation Groups for support (technical, marketing, educational, etc)
- Strong ecosystem for support
- Marketability to a large client base
- Exposure to global markets



Join the Revolution

Stand above the crowd and
innovate on your terms!!



For More Information

RISC-V Foundation Summit



Get Social



@risc_v



risc-v-foundation



riscv.org